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Improvements and Analysis of Neutron Induced Soft Error and Latch-up in High Speed Full CMOS 6T SRAM Products up to 65nm Technology

Soon -Moon Jung, Hoon Lim, Wonseok Cho, Jaehun Jeong, Youngseop Rah , Jaekyun Park, Keunho Lee, Jiyeon Lee, Kyungsik Cha, Chulsoon Chang, Youngchul Jang, and Kinam Kim
R&D Center, Samsung Electronics Kiheung-Eup, Yongin-City, Kyungki-do, Korea ,
82-31-209-4708 sm1116.jung@samsung.com

Introduction

As the operation voltage and the dimensions of memory chips are scaling down, it increases the possibility to face the serious reliability issues by radiation damages of energetic particles such as neutron, proton and alpa particles.

Especially, Full CMOS 6T SRAM is getting more vulnerable due to the existence of inherent dual well structure in a SRAM cell. The dual well (N-well/P-well) makes the parasitic bipolar devices that can be trigged by the radiation induced electrical charges. For example, the space between the wells is 0.12um for SRAM cell of 65nm technology. It causes the device more susceptible to the latch-up event resulted from the radiation induced charge collection rather than SEU (Soft Error Upset). The latch-up event can cause a deadly failure of the memory and the system as shown in Fig.1, the fail bit map after the latch-up being trigged. The soft error upsets are also becoming serious due to the reduction of the critical charges (Qc) for data upset events caused by cosmic neutrons and alpha particles as the operation voltage is reduced and the memory density is increased, compared with DRAM [1].

Therefore, in this study the susceptibility to the neutron induced latch-up event and soft error upsets was investigated in various technologies and various memory cell array schemes to find out the best solution for the SRAM cell design . Both of accelerated beam radiation tests and simulations were used to determine the rate of the latch-up and the soft error rates of the SRAM products.

Experimental Procedure

In order to evaluate the trends of cosmic ray induced failures, such as latch-up and soft error upset in various SRAM technologies , the SRAM products of the various technology were examined with the WNR continuous spectrum neutron source at Los Alamos National Laboratory and mono-energetic neutron beam at KIRAMS in Korea.

In addition to the measurements, the simulation for the latch-up and soft error upsets was performed to investigate the sensitivity to the process and the design of SRAM cell arrays. The well structures of the full CMOS SRAM cell were varied to three ways, such as twin well, deep N-well, P+ epi layer as shown in Fig.3. In order to improve the SER, the process and cell array designs were changed in various ways, such as p+ epi wafer, every cell well biasing, and node capacitor. The simulations and the measurements were simultaneously performed for various technologies and the split conditions.

Neutron Induced Latch-up

For the cell latch-up simulation, the device structure was simulated with TSUPREM IV as shown in Fig3 . Also, the device simulator, MEDICI was used to simulate the latch-up phenomena by electron -hole pair generation and injection. The electron–hole generations, which could be generated by the radiation under the real environment, was simulated by the photo generation method in the simulation tool. For example, the recoil energy loss was assumed 4.0E6eV/um for the neutron radiation. It was assumed that that energy could create charges of 0.17pC/um. Same amount of the electron-hole pairs were injected into the device structures in the simulator. Then the current flow path and the amount were investigated as shown in Fig 4. For example, when the well resistance is high as case(b) in Fig 4 , the current is still measured constantly high after enough period of time has passed. It means that the latch-up is trigged and the hold current is maintained in the simulated condition. With such method the sensitivity of the well structures to the latch-up were simulated. The P+ epi layer has the best immunity to the latch-up. And the deep N-well can improve the latch-up immunity compared with the twin well. It was confirmed in the accelerated neutron beam measurements of the SRAM products in Fig.7. As the dimensions are shrunk, the susceptibility to latch-up was diminished dramatically by reducing N-well and P-well resistances and designing power lines properly in a SRAM cell array.

Neutron Induced Soft Error Rate

As the technology node advances, the SER (Soft Error Rate) is supposed to increase due to reduction of the node capacitance, increase of the bit density, and scaling down of operation voltage. For various technology nodes, the neutron induced SER were measured with WNR beam at Los Alamos laboratory and compared in Fig.9. The measured SER per mega bits are kept almost same for all technologies. Also, the SER values were simulated based on the measured cell node capacitances. The simulated values are matched well with the measured ones as shown in Fig.10.

The SRAM cell node capacitance decreases as the technology node advances. The soft error rates per mega bits are saturated at near several hundreds FIT/Mbit without the MIM capacitor. However, if the node capacitance can be increased or kept constant compared with that of the previous generation of cell, the SER per Mega bits can be decreased. In this reason, W/ SiN / TiN and W/Ta_2O_5/TiN MIM (Metal Insulator Metal)capacitor were formed on the top of the SRAM cell node. (Fig.11) Therefore, the implementation of the MIM capacitor can reduce the SER by almost 1 order according to the SER simulation. In the measurements it was also confirmed that it could be reduced to 1/5 of the failure rates of the SRAM products without the MIM capacitor as shown in Fig.12. However, the SER is not sensitive to the well structure.

Conclusion

We had observed the trends of the neutron induced latch-up and soft error failure rate in SRAM products. From those trends the critical factors, which can reduce both of the failures in the SRAM of 65nm technology, are found.

References

[1] “The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction ’’ R.Baumann. IEDM, 2002. Tech. Dig., p329

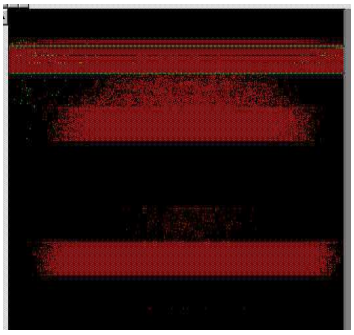

Fig.1 Fail bit map after the latch-up is trigged by neutron radiation in a SRAM. The red ones are the failed bits.

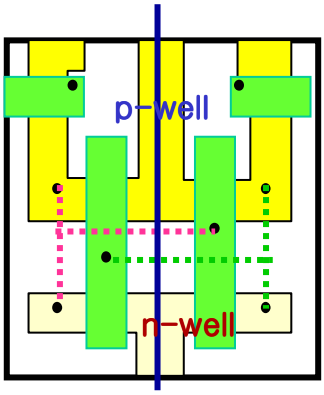

Fig.2 The SRAM cell layout shows the dual well structure of P-well and N-Well in a SRAM cell.

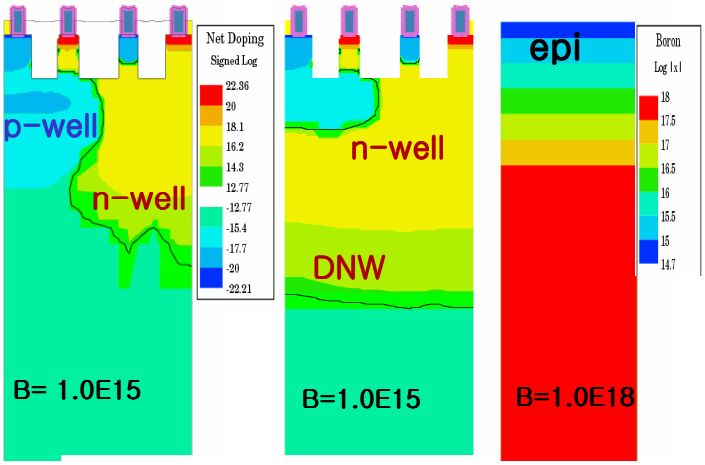

Fig.3 Simulated doping profiles of each well structure (a) twin well,, (b) Deep n-well, and (c) p+-epi wafer in TSUPREM IV simulator .

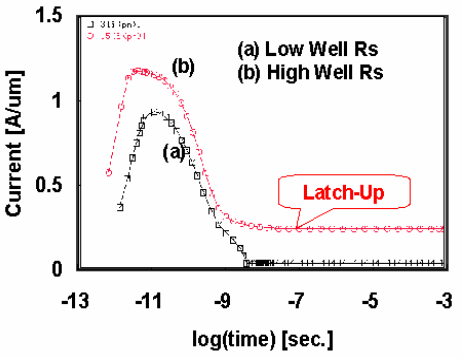

Fig.4 The simulated current after electron-holes generation in the simulated SRAM cell for latch-up

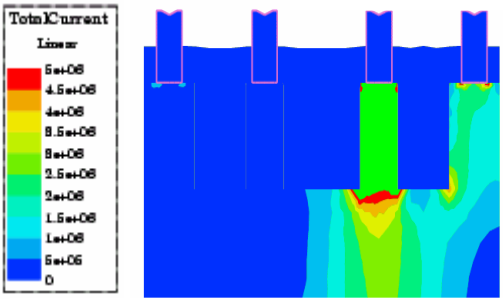

Fig.5 Simulated spatial current flow path in a SRAM cell with the twin well structure at the case of Fig.4(a) in MEDICI simulator.

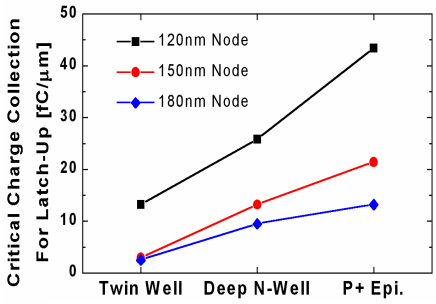

Fig.6 The critical charge collection for latch-up in each well structure for various technology nodes.

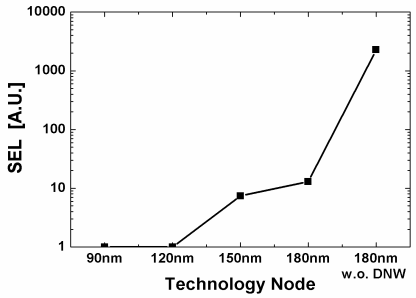

Fig.7 Measured neutron induced Single Event Latch-up failure rate (FIT) for various technology node SRAM at Los Alamos Lab. At the 180nm node with and without Deep N-well

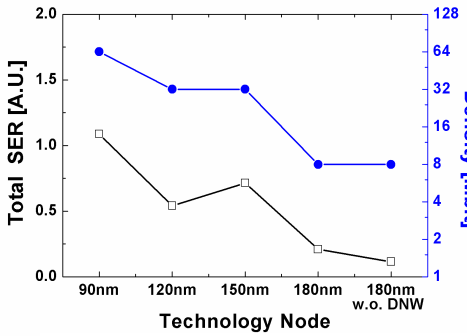

Fig.8 Measured neutron induced soft-error rate(SER) for various technology node SRAM products with WNR beam at Los Alamos

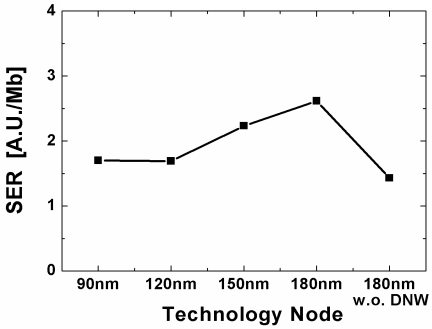

Fig.9 The measured total SER values are expressed as SER per mega-bits. The failure rate is saturated as shown in the graph .

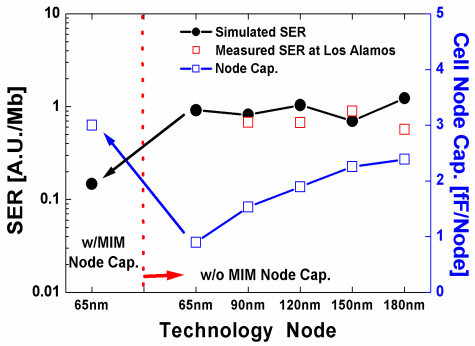

Fig.10 Soft-error rate and node capacitance of SRAM cell as a function of technology node and existence of MIM capacitor.

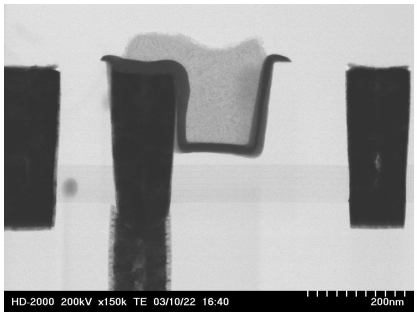

Fig.11 Vertical TEM photograph of MIM node capacitor in a SRAM Cell.

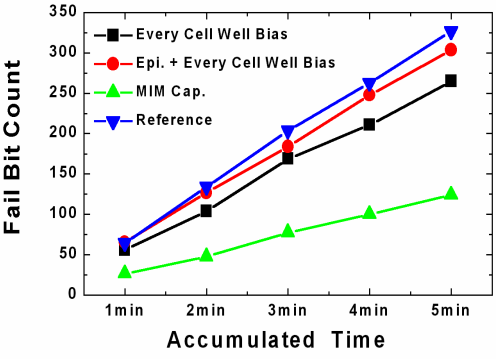

Fig.12 Neutron induced failure rates are measured for the various cell array structures in 64M bits SRAM with 35MeV mono-energetic neutron beam up to 5min. exposure.