A Novel Dual-Metal Gate Integration Process for Sub-1nm EOT HfO₂ CMOS Devices

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1. Introduction

Dual metal gate electrodes on high K gate dielectrics with EOT less than 1 nm is required for aggressively scaled CMOS [1]. Recently, TiN/HfO₂ and HfN/HfO₂ gate stacks with sub-1nm EOT [2,3] have been demonstrated. Although dual metal gates on SiO₂ and HfO₂ gate dielectrics with larger EOT have been reported [4-7], process integration of dual metal gate/high-K gate stack still faces severe challenges, especially in achieving sub-1nm EOT with appropriate metal gate work functions. In this paper, we report and demonstrate a novel approach to implement dual metal gate electrodes into HfO₂ CMOS devices with EOT<1nm and excellent reliability using a HfN dummy metal gate.

2. Experimental

Fig.1 presents the process flow for the dual metal gate CMOS integration with HfO₂ dielectric. First, HfN/HfO₂ gate stack was fabricated using the conventional gate-first CMOS process detailed in [2]. HfN metal gate is essential to achieve EOT<1nm and high carrier mobility after high-temperature S/D annealing [2]. DHF (HF: H₂O = 1:100) was then used to selectively remove the dummy HfN gate electrode without attacking underlying HfO₂ gate dielectric. This critical step takes advantage of extremely high etching selectivity between HfN and HfO₂, as shown in Fig. 2. Finally two other metal electrodes (Ta and Ni in this work) with appropriate work functions for n- and p-MOS were re-deposited on HfO₂. The work function, leakage, and TDDB reliability of the resulting Ta/HfO₂ and Ni/HfO₂ gate stacks are evaluated and compared with initial HfN/HfO₂ gate stack to study whether the selective HF etching would cause any degradation to the underlying HfO₂ gate dielectric.

3. Results and Discussion

Figs. 3-5 show the C-V, the gate leakage, and the effective electron mobility measured on n-MOS devices with TaN/HfN/HfO₂ gate stack fabricated using the gate-first process. The S/D activation was done at 950°C for 30 sec. The gate leakage and peak electron mobility are compared with the recently reported data [3,6,8]. As can be seen, HfN/HfO₂ gate stack shows excellent thermal stability with EOT<1nm, low gate leakage, and high electron mobility. However, the work function of HfN metal gate is close to Si mid-gap position, resulting high threshold voltage for transistors. To integrate dual-metal gates with the high-quality ultra-thin HfO₂ dielectric, the feasibility of using HfN as a dummy gate electrode was investigated. Firstly we evaluated the impact of selective DHF etching of HfN on the quality of underlying HfO₂ dielectrics. Fig. 6 compares AFM surface morphology of the as-deposited HfO₂, 1000°C RTA treated HfO₂, and the HfO₂ in HfN/HfO₂ stack with HfN removed by DHF after 1000°C RTA treatment. As can be seen, DHF removal of HfN does not cause any damage to the underlying HfO₂. To further examine the potential damage to the electrical properties of HfO₂ by DHF removal of HfN from HfN/HfO₂, HfN was re-deposited on HfO₂ after the removal of dummy HfN layer from HfN/HfO₂. Figs. 7-8 compare the C-V, and I-V characteristics between the “control” HfN/HfO₂ device (EOT~0.8nm) that has not received DHF and the device with “re-deposited” HfN on HfO₂ after DHF removal of HfN from the “control” HfN/HfO₂ device. Note that all “control” HfN/HfO₂ devices received 1000°C post-metal annealing. Negligible variation in C-V and leakage between “control” and “re-deposited” devices indicates that the DHF etching process is damage-free to the underlying HfO₂. Dual-metal gates (Ta for n-MOS and Ni for p-MOS) were then deposited on HfO₂ after etching of HfN dummy gate from HfN/HfO₂ stack. Fig. 9 compares high frequency C-V curves between the “control” HfN/HfO₂ (EOT ~ 0.9nm) and the device with “re-deposited” Ni metal gate. Compared to control HfN/HfO₂ devices, Ni/HfO₂ devices show identical EOT with a substantial flat-band voltage (V_fbs) shift (~0.45V) which is attributed to the work function difference between Ni and HfN. Similar phenomena is also observed between control HfN/HfO₂ and re-deposited Ta/HfO₂, as shown in Fig. 10. The work function is determined to be ~4.3 eV for Ta/HfO₂ (n-MOS) and ~5.1eV for Ni/HfO₂ (p-MOS) by taking reference to the mid-gap work function value of HfN (~4.65eV) [2]. A work function difference of 0.8eV between n- and p-MOS is obtained, adequate for dual metal gate CMOS bulk and SOI device applications [5]. Fig.11 shows the gate leakage of the HfO₂ devices with “control” HfN gate, as well as “re-deposited” Ta, Ni, and HfN gate, versus the EOT. Fig. 12 compares the TDBD characteristics among these devices. No observable leakage increase and TDBD degradations in all the “re-deposited” devices after dummy HfN process suggest that this approach provides a solution for easy integration of dual metals in HfO₂ CMOS with EOT<1nm. Ni/HfO₂ and Ta/HfO₂ devices show significantly smaller leakage than poly/SiO₂ by several orders of magnitude.

4. Conclusion

We have successfully demonstrated a novel and simple approach to implement dual metal gate electrodes into HfO₂ CMOS devices with EOT<1nm. A work function difference of ~ 0.8eV between n- and p-MOS is adequate for the dual metal gate CMOS bulk and SOI device applications. 

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References
Fig. 1 The dual metal gate integration process flow for HfO₂ CMOS with EOT<1nm using HfN as a dummy gate.

Fig. 2 Comparison of the etch rates between HfN and HfO₂ by DHF solution (1:100). The etch process is extremely selective.

Fig. 3 High frequency C-V measurement of nMOS transistor (EOT ~0.95nm), with excellent agreement to the simulation considering QM effect.

Fig. 4 Gate leakage as a function of EOT for HfO₂ MOS devices, including the recently published data. The inset shows the Jg vs. Vg curve of the nMOSFET with EOT=0.95nm.

Fig. 5 Comparison of the peak electron effective mobility measured from the 0.95nm nMOSFET with the recently published data.

Fig. 6 AFM pictures of the HfO₂ film surface. a) As-dep, b) after 1000°C RTA, c) after 1000°C RTA with HfN removal.

Fig. 7. C-V comparison of control HfN/HfO₂ and re-deposited HfN/HfO₂ MOS capacitors.

Fig. 8 I-V comparison of control HfN/HfO₂ and re-deposited HfN/HfO₂ MOSC. No degradation leakage is observed as a result of DHF etching process.

Fig. 9 C-V curves comparison for the control HfN/HfO₂ and re-deposited Ni/HfO₂. Same EOT (~0.9nm) but with 0.45V positive shift in VFB is obtained.

Fig. 10 A 0.8eV work function difference between Ta/HfO₂ (n-MOS) and Ni/HfO₂ (p-MOS) is achieved.

Fig. 11 Leakage current comparison between the control HfN/HfO₂ and re-deposited HfN/HfO₂, Ta/HfO₂, and Ni/HfO₂ devices. No degradation as a result of DHF selective etch.

Fig. 12 TDDB comparison between control HfN/HfO₂ and re-deposited HfN/HfO₂, Ta/HfO₂, Ni/HfO₂ devices. No degradation as a result of DHF selective etching.