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A Novel Dual-Metal Gate Integration Process for Sub-1nm EOT HfO_2 CMOS Devices

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1. Introduction

Dual metal gate electrodes on high K gate dielectrics with EOT less than 1 nm is required for aggressively scaled CMOS [1]. Recently, TiN/HfO_2 and HfN/HfO_2 gate stacks with sub-1nm EOT [2,3] have been demonstrated. Although dual metal gates on SiO_2 and HfO_2 gate dielectrics with larger EOT have been reported [4-7], process integration of dual metal gate/high-K gate stack still faces severe challenges, especially in achieving sub-1nm EOT with appropriate metal gate work functions. In this paper, we report and demonstrate a novel approach to implement dual metal gate electrodes into HfO_2 CMOS devices with EOT<1nm and excellent reliability using a HfN dummy metal gate.

2. Experimental

Fig.1 presents the process flow for the dual metal gate CMOS integration with HfO_2 dielectric. First, HfN/HfO_2 gate stack was fabricated using the conventional gate-first CMOS process detailed in [2]. HfN metal gate is essential to achieve EOT<1nm and high carrier mobility after high-temperature S/D annealing [2]. DHF (HF: H_2O =1:100) was then used to selectively remove the dummy HfN gate electrode without attacking underlying HfO_2 gate dielectric. This critical step takes advantage of extremely high etching selectivity between HfN and HfO_2, as shown in Fig. 2. Finally two other metal electrodes (Ta and Ni in this work) with appropriate work functions for n- and p-MOS were re-deposited on HfO_2. The work function, leakage, and TDDB reliability of the resulting Ta/HfO_2 and Ni/HfO_2 gate stacks are evaluated and compared with initial HfN/HfO_2 gate stack to study whether the selective HF etching would cause any degradation to the underlying HfO_2 gate dielectric.

3. Results and Discussion

Figs. 3-5 show the C-V, the gate leakage, and the effective electron mobility measured on n-MOSFETs with TaN/HfN/HfO_2 gate stack fabricated using the gate-first process. The S/D activation was done at 950^{o}C for 30 sec. The gate leakage and peak electron mobility are compared with the recently reported data [3,6,8]. As can be seen, HfN/HfO_2 gate stack shows excellent thermal stability with EOT<1nm, low gate leakage, and high electron mobility. However, the work function of HfN metal gate is close to Si mid-gap position, resulting high threshold voltage for transistors. To integrate dual-metal gates with the high-quality ultra-thin HfO_2 dielectric, the feasibility of using HfN as a dummy gate electrode was investigated. Firstly we evaluated the impact of selective DHF etching of HfN on the quality of underlying HfO_2 dielectrics. Fig. 6 compares AFM surface morphology of the as-deposited HfO_2, 1000^{o}C RTA treated HfO_2, and the HfO_2 in HfN/HfO_2 stack with HfN removed by DHF after 1000^{o}C RTA treatment. As can be seen, DHF removal of HfN does not cause any damage to the underlying HfO_2. To further examine the potential damage to the electrical properties of HfO_2 by DHF removal of HfN from HfN/HfO_2, HfN was re-deposited on HfO_2 after the removal of dummy HfN layer from HfN/HfO_2. Figs. 7-8 compare the C-V, and I-V characteristics between the "control" HfN/HfO_2 device (EOT~0.8nm) that has not received DHF and the device with "re-deposited" HfN on HfO_2 after DHF removal of HfN from the "control" HfN/HfO_2 device. Note that all "control" HfN/HfO_2 devices received 1000^{o}C post-metal annealing. Negligible variation in EOT and leakage between "control" and "re-deposited" devices indicates that the DHF etching process is damage-free to the underlying HfO_2. Dual-metal gates (Ta for n-MOS and Ni for p-MOS) were then deposited on HfO_2 after etching of HfN dummy gate from HfN/HfO_2 stack. Fig. 9 compares high frequency C-V curves between the "control" HfN/HfO_2 (EOT ~ 0.9nm) and the device with "re-deposited" Ni metal gate. Compared to control HfN/HfO_2 devices, Ni/HfO_2 devices show identical EOT with a substantial flat-band voltage (V_{FB}) shift (~0.45V) which is attributed to the work function difference between Ni and HfN. Similar phenomena is also observed between control HfN/HfO_2 and re-deposited Ta/HfO_2 devices, as shown in Fig. 10. The work function is determined to be ~4.3 eV for Ta/HfO_2 (n-MOS) and ~5.1eV for Ni/HfO_2 (p-MOS) by taking reference to the mid-gap work function value of HfN (~4.65eV) [2]. A work function difference of 0.8eV between n- and p-MOS is obtained, adequate for dual metal gate CMOS bulk and SOI device applications [5]. Fig.11 shows the gate leakage of the HfO_2 devices with "control" HfN gate, as well as "re-deposited" Ta, Ni, and HfN gate, versus the EOT. Fig. 12 compares the TDDB characteristics among these devices. No observable leakage increase and TDDB degradations in all the "re-deposited" devices after dummy HfN process suggest that this approach provides a solution for easy integration of dual metals in HfO_2 CMOS with EOT<1nm. Ni/HfO_2 and Ta/HfO_2 devices show significantly smaller leakage than poly/SiO_2 by several orders of magnitude.

4. Conclusion

We have successfully demonstrated a novel and simple approach to implement dual metal gate electrodes into HfO_2 CMOS devices with EOT<1nm. A work function difference of ~ 0.8eV between n- and p-MOS is adequate for the dual metal gate CMOS bulk and SOI device applications.

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References

[1] ITRS 2002 update, http//public.itrs.net; [2] H.Y. Yu et al., *IEDM'03*, p.99, 2003; [3] W. Tsai et al., *IEDM'03*, p.311, 2003; [4] C.S. Park et al., *2003 VLSI Tech. Dig.*, p149, 2003; [5] J.H. Sim et al., *IEEE Electron Device Lett.*, p.631, 2003; [6] S.B. Samavedam et al., *IEDM'02*, p.433, 2002; [7] J.H. Lee et al., *IEDM'03*, p.323, 2003; [8] B. Guillaumot et al., *IEDM'02*, p.355, 2002

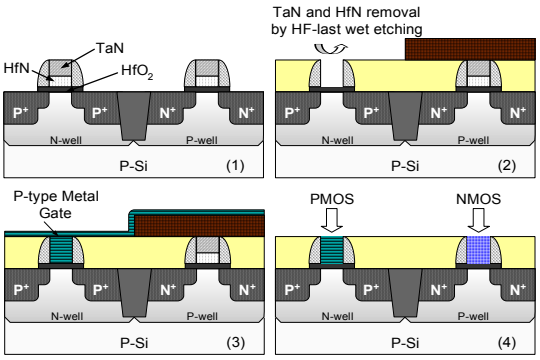

Fig. 1 The dual metal gate integration process flow for HfO_2 CMOS with EOT<1nm using HfN as a dummy gate.

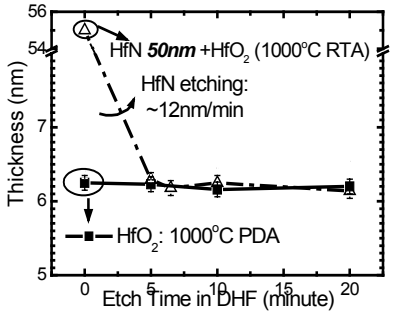

Fig. 2 Comparison of the etch rates between HfN and HfO_2 by DHF solution (1:100). The etch process is extremely selective.

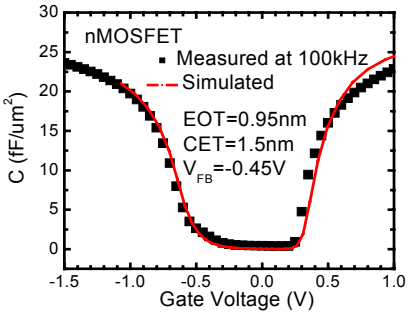

Fig. 3 High frequency C-V measurement of nMOS transistor (EOT =0.95nm), with excellent agreement to the simulation considering QM effect.

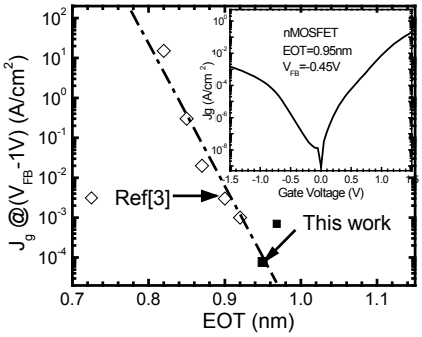

Fig. 4 Gate leakage as a function of EOT for HfO_2 MOS devices, including the recently published data. The inset shows the Jg vs. Vg curve of the nMOSFET with EOT=0.95nm.

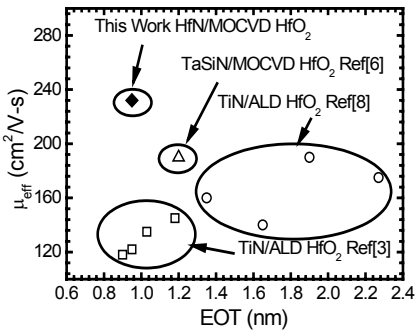

Fig. 5 Comparison of the peak electron effective mobility measured from the 0.95nm nMOSFET with the recently published data.

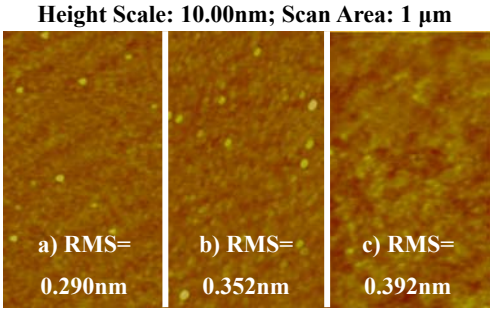

Fig. 6 AFM pictures of the HfO_2 film surface. a) As-dep, b) after 1000°C RTA, c) after 1000°C RTA with HfN removal.

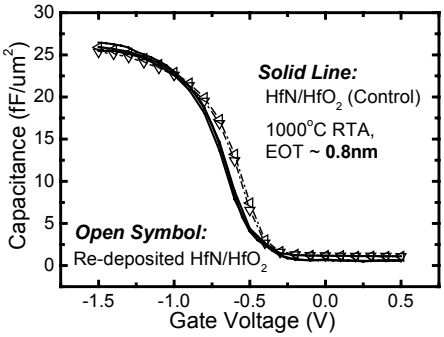

Fig. 7. C-V comparison of control HfN/HfO_2 and re-deposited HfN/HfO_2 MOS capacitors.

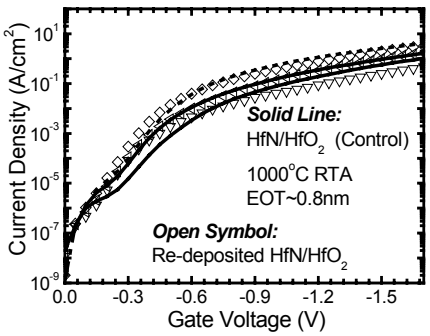

Fig. 8 I-V comparison of control HfN/HfO_2 and re-deposited HfN/HfO_2 MOSC. No degradation leakage is observed as a result of DHF etching process.

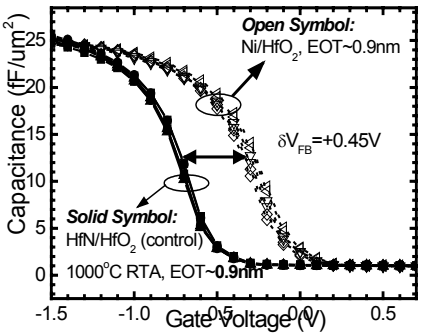

Fig. 9 C-V curves comparison for the control HfN/HfO_2 and re-deposited Ni/HfO_2. Same EOT (~0.9nm) but with 0.45V positive shift in V_{FB} is obtained.

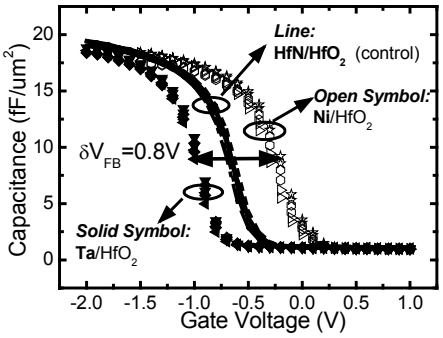

Fig. 10 A 0.8eV work function difference between Ta/HfO_2 (n-MOS) and Ni/HfO_2 (p-MOS) is achieved

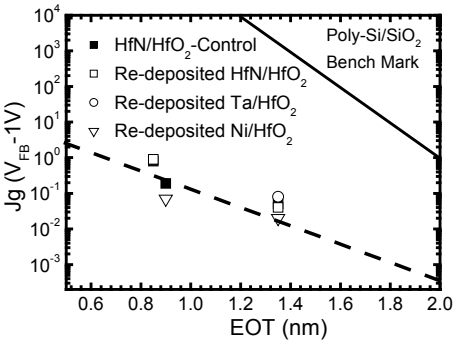

Fig. 11 Leakage current comparison between the control HfN/HfO_2 and re-deposited HfN/HfO_2, Ta/HfO_2, and Ni/HfO_2 devices. No degradation as a result of DHF selective etch.

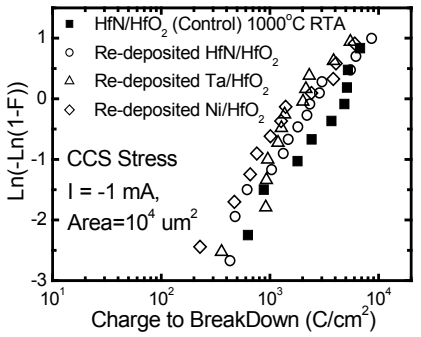

Fig. 12 TDDB comparison between control HfN/HfO_2 and re-deposited HfN/HfO_2, Ta/HfO_2, Ni/HfO_2 devices. No degradation as a result of DHF selective etching.