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Effect of Fluorine on Interface Characteristics in Low-temperature CMIS Process with HfO_2 Metal Gate Stacks

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I. Introduction

In order to improve device performance, thinner gate insulators are required for deep sub-micron MOSFETs. In the situation where a thinner gate insulator is required, high-k dielectrics are effective for suppressing gate leakage current. However, one major issue for applying higk-k dielectrics is the reaction between high-k dielectric and poly-Si, which is called "Fermi Pinning" [1], that results in high threshold voltage for P-ch FETs. Therefore, a metal electrode was proposed in order to prevent the interface reaction. However, high temperature annealing such as a source/drian activation results in a thermal reaction between the metal and the high-k dielectric. In order to avoid this problem, the replacement gate technique[2,3] has been widely used for the fabrication of metal-gate CMIS devices.

In this paper, we report that the interface characteristics between Si substrate and gate dielectric have been improved using F_2 gas annealing that is applicable to a low temperature process in metal-gate CMIS devices.

II. Experiments and Measurements

A. Fabrication Processes

MIS FETs were fabricated using the process flow shown in Fig. 1 (a). A 2.0 nm-thick of SiON was formed by plasma oxidation followed by plasma nitridation. SiN on SiON dielectric was deposited with the cyclic-CVD at 0.2 nm EOT (equivalent oxide thickness) per 10 cycles. The fluorine incorporation process was achieved by F_2 gas annealing before the deposition of poly-Si. F_2 gas annealing at low temperature was carried out in reduced pressure. After the formation of the gate dielectrics, 150 nm poly-Si was deposited on this stack. After patterning the gate electrode, the S/D (source/drain) was implanted and annealed at 1050°C.

Metal gate MIS FETs were fabricated by a replacement gate technique using the process flow shown in Fig. 2 (a). After removing the dummy gate, SiN/HfO_2 gate dielectric stack was newly deposited using ALD (atomic layer deposition) and cyclic-CVD. The thickness of HfO_2 dielectric is 2 nm and cyclic-CVD can deposit SiN on high-k dielectric at 0.2 nm EOT. As the gate electrode, W/TiN gate electrode was deposited by CVD on the SiN/HfO_2 layer.

B. Measurements

The initial interface state density of N-ch and P-ch FETs was measured by charge pumping technique. Moreover, BT stress was applied in the wafer level test, and the stress time was 10000 s. The stress bias was around 10 MV/cm at 125 °C. We discuss NBTI (Negative Bias Temperature Instability) and PBTI (Positive Bias Temperature Instability) as a differential value between the initial threshold voltage (Vth) and Vth after stress.

III. Results and Discussions

A. F_2 Annealing Process

Figure 3 shows AFM (Atomic Force Microscope) results of F_2 gas annealed SiN/SiON gate stacks. From this figure, no roughness is observed. We have confirmed the same morphology in single SiON film. SIMS (Secondary Ion Mass Spectrometry) from Si substrate side results are shown in Fig. 4. The peak concentration of fluorine is $5 \times 10^{20} cm^{-3}$ in case of F_2 annealing process, which has the same profile as BF_2 ion implantation at S/D formation[4]. The CV curves in Fig. 5 indicate the slight decrease of EOT.

B. Effect of Fluorine on Nit and NBTI

Figure 6 shows two cases of the enhancement for fluorine effect i.e., one is caused by highly doped fluorine in the gate dielectrics, and the other is caused by the cyclic-SiN that contains hydrogen that originated in the material gas. The interface state (Nit) of gate stacks to which F_2 gas annealing process has been applied is decreased for both cases of with or without cyclic-SiN This result is consistent with that in the previous literature [4]. The ΔVth (NBTI) for P-channel FETs was reduced in case of F_2 gas annealing process. These results are the proof that the fluorine in the interface region is effective for the improvement of the BT instability.

C. W/TiN/HfO_2 Gate Stacks

Figure 7 (a) indicates the effect of Nit using F_2 gas annealing process in W/TiN/SiN/HfO_2 gate stacks. In the low temperature process, interface state density is significantly large as compared with Nit in the SiON process. In the case of W/TiN/SiN/HfO_2 gate stack to which F_2 gas annealing was applied , Nit was smaller than that without F_2 gas annealing. Figure 7 (b) shows ΔVth (NBTI) for P-channel FETs and ΔVth (PBTI) for N-channel FETs that have the W/TiN/SiN /HfO_2 gate stacks. NBT for P-channel FET shows the advantage of the F_2 process. However PBT for N-channel FETs doesn't show the improvement of the instability in spite of F_2 gas annealing. Both the cases indicate that the bulk charge trap in the high-k film is a major cause of PBT degradation. Contrary to SiON gate stacks, the instability of HfO_2 gate stacks was mainly determined by bulk charge trap.

IV. Conclusion

A study of the effects of fluorine on the interface characteristics has been presented. The interface states in the SiON film can be decreased using F_2 gas annealing process. NBTI is dramatically improved by fluorine and hydrogen at the interface region. In case of W/TiN/HfO_2, PBTI has not changed even if annealed with F_2 gas, in spite of the decrease of Nit. Suppressing both traps at interface and in bulk is important for the low temperature process of high-k metal MIS FETs.

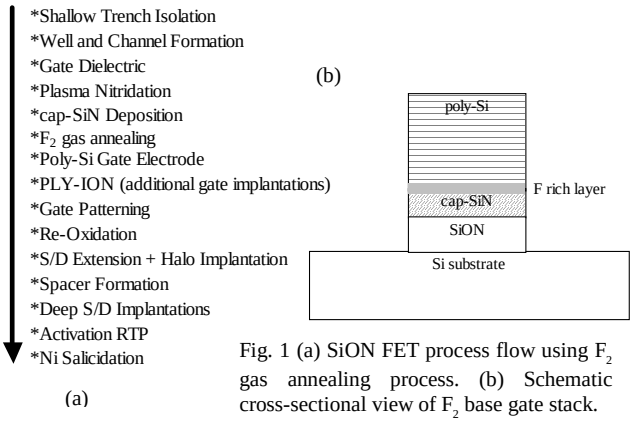

Fig. 1 (a) SiON FET process flow using F_2 gas annealing process. (b) Schematic cross-sectional view of F_2 base gate stack.

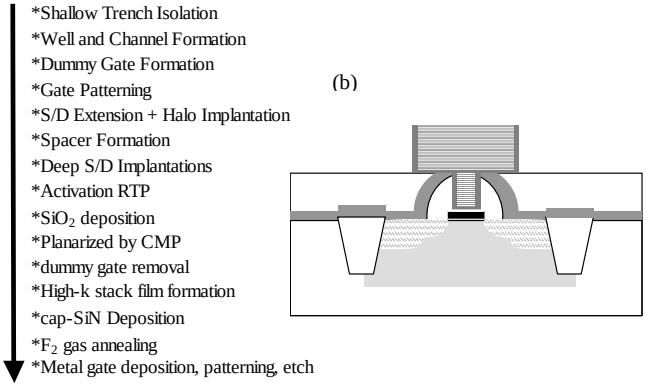

Fig. 2 (a) Replacement gate process flow for SiN/HfO_2 gate dielectrics. (b) Cross-sectional device structure of the replacement MIS-FET.

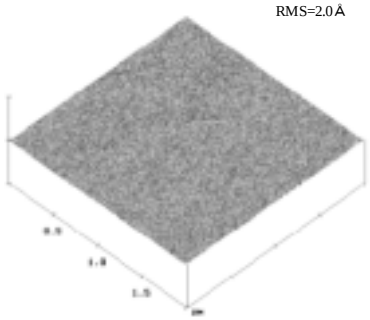

Fig. 3 AFM image of SiON and cyclic-SiN stack after F_2 gas annealing process.

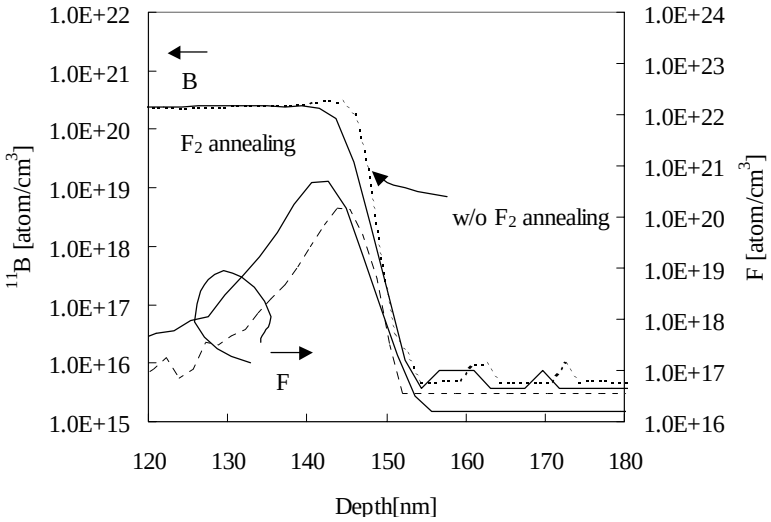

Fig. 4 SIMS profiles of boron and fluorine. Solid lines show SiON film profile with F_2 gas annealing. Dashed lines are without F_2 gas annealing.

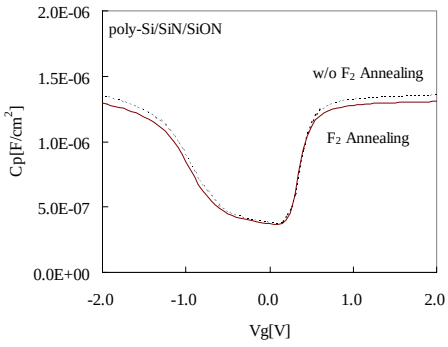

Fig. 5 N-ch FET capacitance curve for both cases of with or without F_2 gas annealing in SiN/SiON MIS FETs

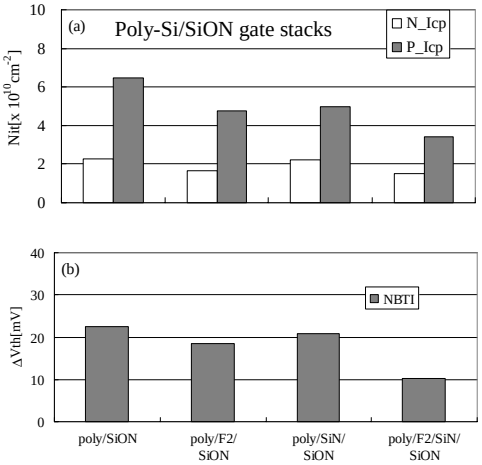

Fig. 6 Nit and NBTI under several gate stacks. (a) Nit for N-channel FET and P-ch FET. (b) ΔVth for P-channel FET defiiend as 10 MV/cm at 125 °C

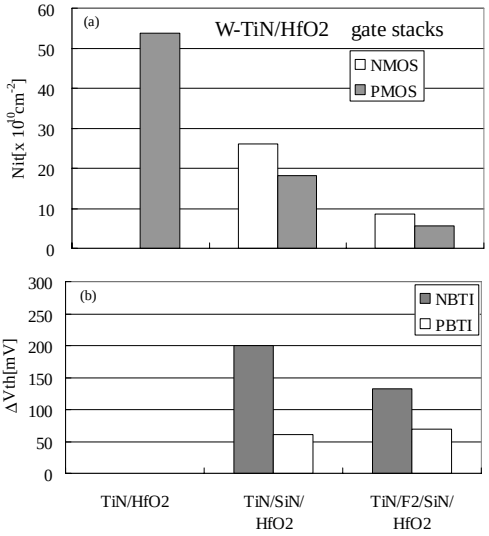

Fig. 7 W-TiN/HfO_2 or W-TiN/SiN/HfO_2 gate stacks.
(a) Nit decreasing effect of cyclic-SiN and F_2 process for N-channel FET and P-channel FET.
(b) ΔVth after 10000 sec under the 10 MV/cm stress condition. NBTI for P-channel FET is significantly decreased using F_2 process.

References
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