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Behavior of Effective Work Function in Metal/High-K Gate Stack under High Temperature Process

Moon Sig Joo, Byung Jin Cho*, D. Z. Chi[1], N. Balasubramanian[2], and D.-L. Kwong[3]

Silicon Nano Device Laboratory, Dept. of Electrical & Computer Engineering, NUS, Singapore 119260, Phone: 65-6874-6470

Fax: 65-6779-1103, *email: elebjcho@nus.edu.sg, [1]Institute of Materials Research & Engineering, Singapore 117602,

[2]Institute of Microelectronics, Singapore 117685, [3]Dept. of ECE, University of Texas, Austin, USA

Abstract

Thermal instability of effective work function and its material dependence on metal/high-K gate stack is investigated. It is found that thermal instability of the effective work function of metal electrode on gate dielectric is strongly dependent on gate electrode and dielectric material. Thermal instability of metal gate is related to the presence of silicon at the interface and the Fermi-level pinning position is depending on the location of silicon at the interface.

Introduction

Aggressive scaling of CMOS devices requires the metal gate electrode on high-K dielectrics in near future. The effective work functions ($\Phi_{m,eff}$) of metal gates on high-K dielectrics are different from their vacuum work functions ($\Phi_{m,vac}$) and the relationship varies for different dielectrics [1-4]. The behavior of $\Phi_{m,eff}$ on high-K, especially the dependence of gate materials and its thermal instability, is still poorly understood. In this paper, we report new findings on the thermal instability of $\Phi_{m,eff}$ of metal/high-K stack and its material dependence.

Experimental

HfAlO films were deposited on the DHF-cleaned Si-substrate by MOCVD [5], followed by post deposition annealing (PDA) at 700ºC for 1 min. Three metal nitride electrodes, HfN, TaN, and TaSiN were deposited for gate electrode using reactive sputtering. For comparison, MOCVD HfO_2 and pure thermal SiO_2 were also prepared. For thermal stability study, RTA at 700 ~ 950 ºC for 30 sec were done after gate pattering. Post metallization annealing (PMA) in a forming gas ambient was done to all devices.

Results and discussion

Figure 1 shows $\Phi_{m,eff}$ vs. $\Phi_{m,vac}$ for several metals on HfAlO, HfO_2, and SiO_2. The experimental slope parameter S and the charge neutrality level (Φ_{CNL}) are summarized in Table 1. S and Φ_{CNL} values of HfAlO film lie in between those of SiO_2 and HfO_2, which indicates weaker Fermi-level pinning compared to HfO_2. The values obtained are comparable to the theoretical ones predicted by metal-induced gap states (MIGS) theory [1-4]. These values were obtained from the samples without any high temperature process except PMA, and therefore can be said the intrinsic properties of the materials. However, in actual CMOS devices which require high temperature annealings in the fabrication procedure, these values are not applicable in prediction of V_t because of thermal instability of $\Phi_{m,eff}$ on high-K. The behavior of $\Phi_{m,eff}$ of metal nitrides on HfAlO after annealing is investigated. Fig. 2 shows a plot of V_{fb} vs. EOT for three different metal nitrides on HfAlO before high temperature RTA. All lines are parallel, showing that initial charges in HfAlO are the same. After RTA, however, the $\Phi_{m,eff}$ and charges are strongly depending on electrode materials (Fig. 3). For HfN and TaN on HfAlO, the charge in the HfAlO changes from negative to positive as the annealing temperature increases, but the extrapolated lines are merging to almost a single point, indicating that there is no obvious change in $\Phi_{m,eff}$. For TaSiN, however, the dielectric charges are maintained almost the same but $\Phi_{m,eff}$ significantly decreases towards E_C level of silicon as the annealing temperature increases (Fig. 4b) [6], [7]. Because of this strong dependence of $\Phi_{m,eff}$ on electrode materials after annealing, the data points in the plot of $\Phi_{m,eff}$ vs. $\Phi_{m,vac}$ do not fall on a straight line (Fig. 5), indicating that MIGS theory with intrinsic interface states is not applicable after annealing. This is believed to be due to the generation of extrinsic interface states at the metal/high-K interface. The modification of $\Phi_{m,eff}$ after annealing is found not only on high-K but also on SiO_2, too (Fig. 6) [8]. For SiO_2, the $\Phi_{m,eff}$ values are increasing with temperature, which is the opposite direction of the case of TaSiN/HfAlO.

A very interesting phenomenon can be found if the data in Fig. 3-6 are carefully examined. The modification of $\Phi_{m,eff}$ after annealing happens only when "silicon" is present at the metal/dielectric interface, no matter where silicon is, either in dielectric or in gate material. But the direction of $\Phi_{m,eff}$ change is depending on the location of silicon. When silicon is at the gate electrode side (like TaSiN/HfAlO stack), $\Phi_{m,eff}$ decreases after annealing, which means that the extrinsic interface states generated by Si-M bond are located near to E_C of silicon, causing Fermi-level pinning at near E_C of silicon. In Ref [9], poly-Si/HfO_2 stack also shows the same trend of Fermi-level pinning, which also can be explained by the location of silicon (electrode side). When silicon is at the dielectric side (like TaN/SiO_2 stack), $\Phi_{m,eff}$ increases after annealing, indicating the extrinsic interface states are located near to E_V of silicon. When there is no silicon involved, no thermal instability in $\Phi_{m,eff}$ is observed, which means no additional generation of extrinsic interface states by annealing.

In order to have further confirmation on the effect of silicon, we intentionally incorporated silicon atoms to the interface of TaN/HfAlO stack and monitored the behavior of $\Phi_{m,eff}$ after annealing. Silicon incorporation onto the top surface of HfAlO was implemented by silicon passivation (SP) technique using SiH_4 gas flow at 450ºC for 1 minute. The silicon incorporation into HfAlO was confirmed by XPS analysis as shown in Fig. 7. Fig. 8 shows the behavior of $\Phi_{m,eff}$ of TaN/silicon-passivated HfAlO stack after annealing. The $\Phi_{m,eff}$ obviously increases after annealing, which is not observed in TaN/HfAlO without SP. The $\Phi_{m,eff}$ value is merged to around 4.8 eV, similar to the cases of HfN/SiO_2 and TaN/SiO_2 stacks. This result clearly verifies the role of silicon to the instability of $\Phi_{m,eff}$ during high temperature annealing.

Conclusions

Thermal instability of $\Phi_{m,eff}$ of metal/high-K gate stack shows a strong material dependence of both metal electrode and dielectric. It has been found that the presence of silicon and its location at the interface plays a major role in the modification of $\Phi_{m,eff}$ after annealing.

References

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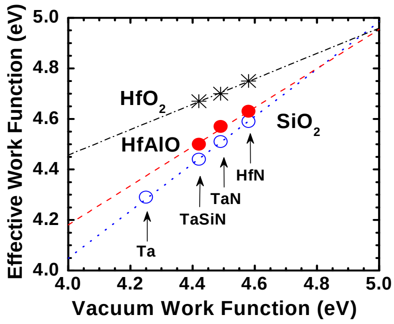

Fig. 1. $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ for various gate dielectrics. HfAlO and HfO_2 show higher $\Phi_{m,eff}$ values than SiO_2 does.

Dielectric	Φ_{CNL} (eV)	S (This work)	S (MIGS)
SiO_2	4.7	0.95[a]	0.86
HfO_2	4.9	0.50	0.53
HfAlO	4.8	0.77	0.63

[a] Taken from Ref [4].

Table 1. Comparison of theoretical and experimental slope parameter S and Φ_{CNL} under three metal nitride gate electrodes.

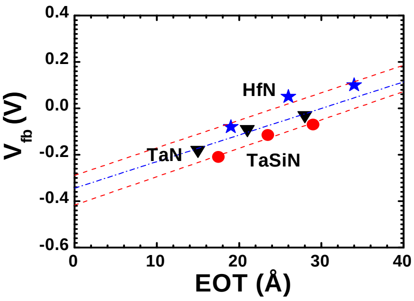

Fig. 2. V_{fb} versus EOT for HfAlO film under three metal nitrides. Initial charges in HfAlO films are the same for three different metal electrodes.

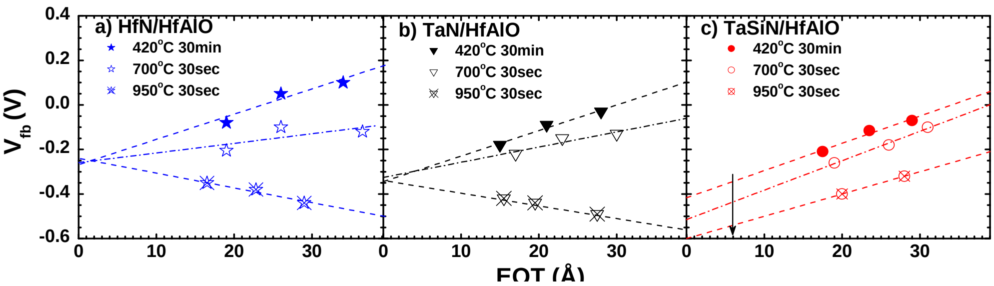

Fig. 3. V_{fb} versus EOT for (a) HfN, (b) TaN and (c) TaSiN on HfAlO after annealing at different temperatures. Both HfN and TaN show the change of dielectric charge whereas TaSiN on HfAlO shows the change of work function after high temperature anneal.

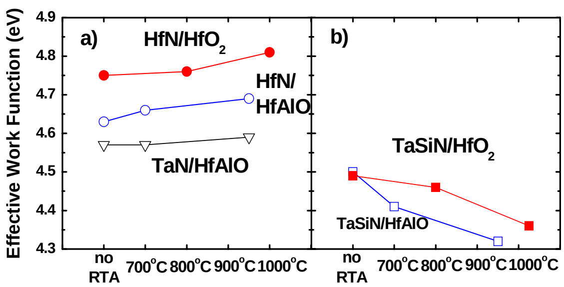

Fig. 4. (a) (b) Thermal instability of $\Phi_{m,eff}$ of metal nitride electrodes on HfAlO and HfO_2. The work functions for TaSiN approaches E_C of silicon after RTA. Data for HfN/HfO_2 and $TaSiN/HfO_2$ were taken form Ref. [6] and [7], respectively.

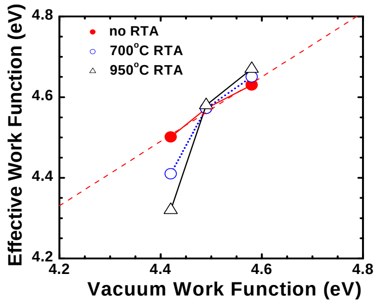

Fig. 5. $\Phi_{m,eff}$ vs. $\Phi_{m,vac}$ on HfAlO after annealing at different temperatures. The result indicates that MIGS theory with intrinsic interface states is not applicable after annealing.

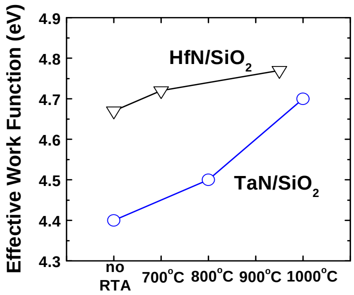

Fig. 6. $\Phi_{m,eff}$ after annealing for HfN and TaN on SiO_2. The $\Phi_{m,eff}$'s for both electrodes increase after high temperature RTA. Data for TaN/SiO_2 were taken from ref [8].

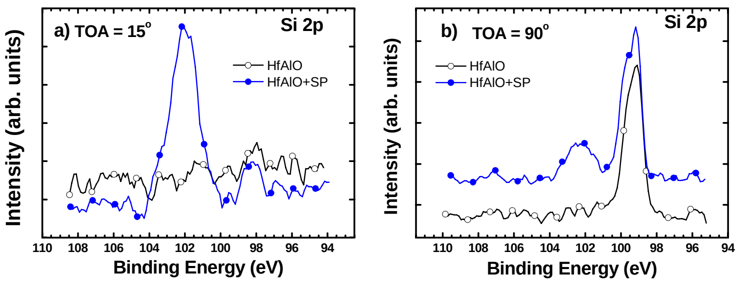

Fig. 7. Si 2p core-level spectra at two different take-off angles of (a) 15° and (b) 90°. Compared to HfAlO without SP, Si-passivated HfAlO sample shows strong peak at around 102.3 eV, which indicates Hf silicate bond (Hf-O-Si).

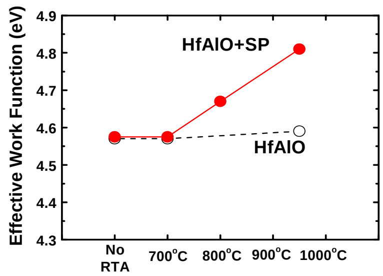

Fig. 8 Thermal instability of $\Phi_{m,eff}$ of HfAlO sample with SP. $\Phi_{m,eff}$ value approaches around 4.8 eV as RTA temperature increases.