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Suppression of Gate Depletion in p+ Polysilicon Gated Sub-40nm PMOS Devices by Laser Thermal Process

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Introduction

For aggressively scaling of CMOS devices, thinner gate oxide is required, and at the same time, suppression of gate depletion is also important. Low thermal budget source-drain rapid thermal annealing (SD-RTA) processing becomes more important to maintain shallow junctions for well-controlled short channel effects. However, low thermal budget SD-RTA tends to induce severe poly-Si gate depletion due to low dopant diffusivity and activation and, as a result, device performance is degraded. Thus, gate pre-doping and pre-annealing technique becomes more important to control thermal budget for SD annealing independently [1,2]. Fig. 1 shows the electrical inversion oxide thickness and threshold voltage (Vth) shift as a function of gate annealing conditions for p+ poly-Si gated PMOSFET as an example. By applying gate pre-annealing, gate depletion is clearly suppressed and higher annealing temperature is more effective due to higher dopant diffusion and activation. However, at the same time, high temperature annealing tend to induce the positive shift of Vth due to boron penetration through the gate oxide and into the channel region. In our experiments, 0.01nm improvement requires 80mV of Vth shift (see low to high temperature). This implies that suppression of gate depletion and boron penetration, which causes performance degradation, Vth variation and reliability issues tend to fall into the relations of the trade-off. Recently, gate activation by laser thermal process (LTP) has been reported [3], and its characteristics of sub-40nm MOSFETs have also been reported [4,5]. In this paper, we report, for the first time, that LTP as a gate pre-annealing is superior to RTA for both gate activation and suppression of boron penetration.

Experimental

Fig. 2 shows the concept of gate activation by LTP. We have demonstrated that the source-drain extension (SDE) profiles and deep source-drain profiles formed by LTP to reduce the parasitic resistance and improve device performance [6,7]. In previous work, we focused on selective melting for recrystallization and dopant profile control, which was realized with pre-amorphization ion implantation. This is based on the fact that the melting point of amorphous-Si is lower than the melting point of single crystal-Si. In this work, we used amorphous-Si as the gate material for selective melting to recrystallization [4,5]. Doped amorphous-Si is transformed to poly-Si and highly activated dopant profiles down to gate / gate oxide interface can be achieved by selective melting to recrystallization. Fig. 3 shows the SIMS profiles of boron concentration using various laser power conditions. Ion sputtering at SIMS measurement is from the sample surface, and the sample structure is also shown in Fig. 3. As can be seen, higher laser power induces deeper boron profile. This implies that boron shows very high diffusion in the melting region, so if we select suitable laser power condition, higher concentration at the gate / gate oxide interface can be obtained without inducing boron penetration into the gate oxide. Fig.4 shows the TEM image of boron implanted amorphous Si on gate oxide after 0.8[J/cm^2]. We can see that amorphous Si is transformed to poly-Si completely. The related SIMS profile (shown in the right of Fig. 4) confirms that boron diffuses down to gate / gate oxide interface. And, higher boron concentration can be obtained at the gate / gate oxide interface after spike-RTA (SD-RTA is presumed this), so we have selected the power of 0.8[J/cm^2] for device fabrication.

Device Fabrication

The fabrication process flow of LTP MOSFETs is shown in Fig. 5. After device isolation with shallow trench isolation (STI), a conventional well is formed followed with a threshold voltage control implantation. A nitrided oxide is used as the gate insulator. For the LTP device, amorphous Si is deposited as the gate electrode material and is transformed to poly-Si with highly activated dopant profiles after laser annealing by melt to recrystallization. For RTA device as a control device, poly-Si is deposited. We have chosen optimized RTA condition for gate activation, and boron implantation dose is ten times lowered compared to LTP device for the suppression of boron penetration. A spike RTA is performed with high ramp-up/down rate as the SD-RTA and its peak temperature is comparatively lowered for the effective suppression of short-channel effects. We applied low thermal budget side-wall CVD and BEOL process for the suppression of dopant deactivation [5].

Result and Discussion

IonIoff characteristics of RTA (with poly-Si), LTP and no LTP (with amorphous-Si) are compared in Fig. 6. We see the Ion current is improved drastically with the use of LTP, while very poor performance is observed for the case of no LTP because of severe gate depletion. Moreover, 4% of Ion current improvement to RTA device can be obtained (LTP:394μA/μm, RTA:378μA/μm at Ioff=7e-8A/μm). Fig.7 shows the gate capacitance characteristics of long channel PMOSFETs with LTP and RTA. LTP device shows 0.07nm improvement of gate depletion to RTA device. And RTA device shows the positive Vfb shift compared to LTP device due to boron penetration to the gate oxide. Fig. 8 shows the Vth-rolloff characteristics with LTP and RTA. Higher Vth can be seen for LTP device due to the suppression of boron penetration. From the comparison between LTP and RTA devices shown in Fig.7, LTP device shows smaller Ioff current of longer channel transistors than that of RTA device. Fig. 9 shows the Id-Vg and Ig-Vg curves of gate length of 1μm. We can see in this figure that the inversion Ig current is almost the same due to the use of the same gate oxide, and Ig current dominates Ioff current for both LTP and RTA devices. However, LTP device shows smaller off-state Ig current than RTA device. Ig current at off-state bias condition flows mainly through gate to drain overlap region, and it is not depend on the gate length, and depends on the length of drain overlap region [8,9]. In our experiments, conditions of SDE implantation and SD-RTA are all the same for LTP and RTA devices, and no significant difference can be seen for the shape of gate electrode after gate formation etching between LTP and RTA devices. So, SDE overlap length must be the same for LTP and RTA devices. Fig. 10 shows the overlap capacitance and off-state Ig current as a function of gate length for LTP and RTA. No difference can be seen for overlap capacitance (namely SDE overlap length), but larger Ig current can be seen for RTA device. This implies that this larger off-state Ig current of RTA device is not based on drain overlap length. And, as it is seen in Fig. 7, as for no LTP with amorphous gate as well, Ioff current of longer channel transistor is small as well as with LTP. These suggest that this smaller off-state Ig current for LTP device is caused by roughness reduction by use of amorphous Si as a gate material and it reduces local field enhancement as already reported in ref. [10]. Fig. 11 shows the bias temperature stress time dependence of Vth shift for PMOSFETs with LTP and RTA. Though the amount of ten times of boron is implanted for the LTP device, no degradation can be seen at the same stress gate bias condition due to the suppression of boron penetration.

Conclusions

We have demonstrated for the first time that LTP as a gate pre-annealing is superior to RTA for both gate activation and suppression of boron penetration. Higher Ion current by 4% and suppression of gate depletion by 0.07nm can be obtained for LTP with suppressing boron penetration compared to RTA. We confirm that LTP is a very useful technique for the gate activation annealing.

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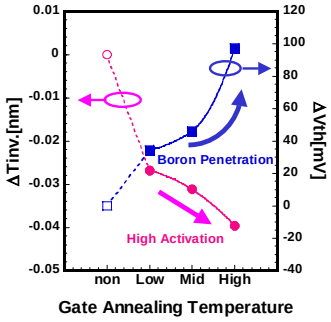


Fig.1. Suppression of gate depletion and Vth shift for various gate annealing conditions for p+ poly-Si gated PMOS.

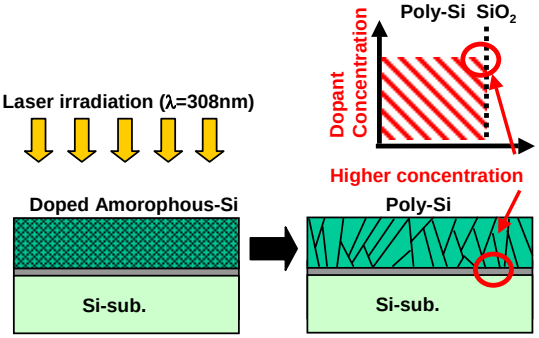


Fig.2. Schematic diagrams of gate activation by laser thermal process (LTP).

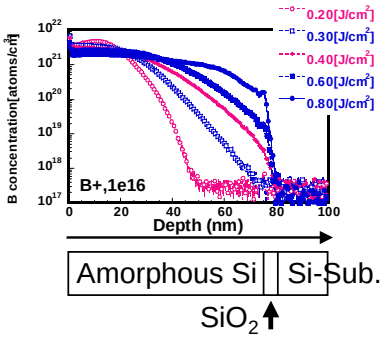


Fig.3. SIMS Profiles of B concentration for various laser power conditons.

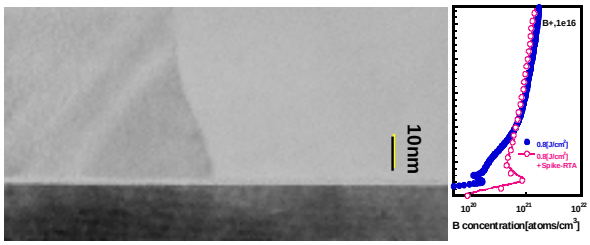


Fig.4. Cross-sectional TEM image of B implanted amorphous Si after 0.80[J/cm²] of laser irradiation, and its SIMS profile of B concentration (right figure).

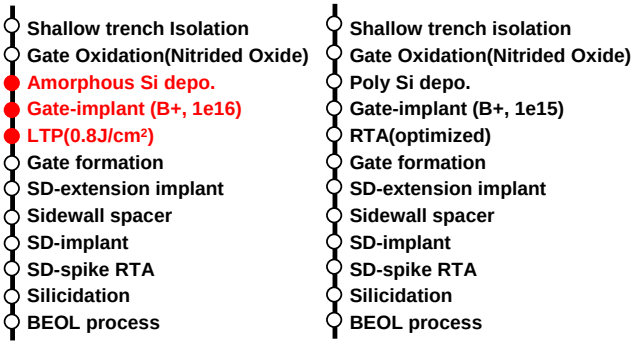


Fig.5. Fabrication process flow of LTP PMOSFET and control device.

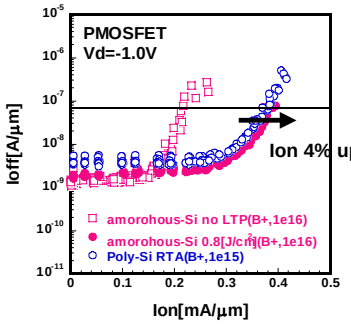


Fig.6. Ionloff characteristics with different gate activation conditions.

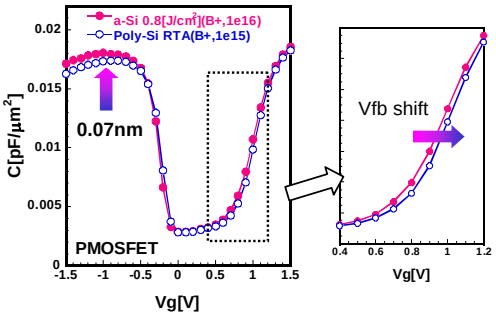


Fig.7. Comparison of gate capacitance with LTP and RTA. The right figure is the expansion figure of the part enclosed with the dotted line of the left figure.

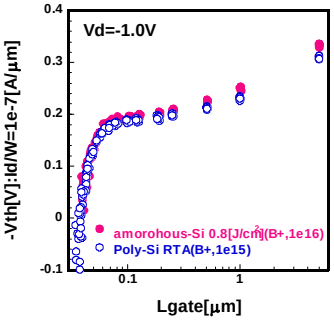
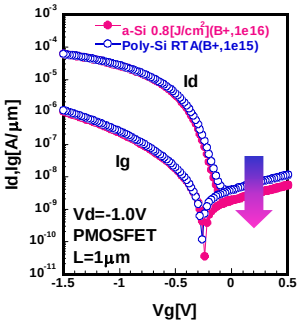
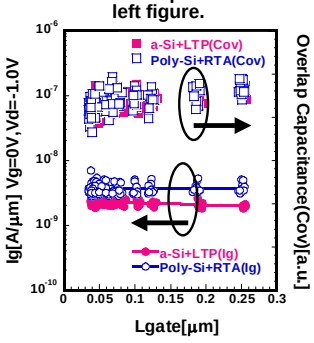


Fig.8. Comparison of Vth-rolloff with LTP and RTA.





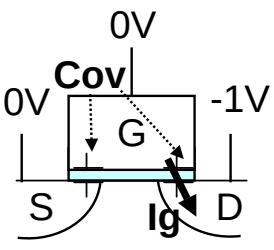


Fig.9. Comparison of Id-Vg, Ig-Vg characteristics with LTP and RTA.

Fig.10. Overlap capacitance (Cov) and off-state Ig current as a function of Lgate for LTP and RTA (Left figure). Righ figure shows the schematic illustration of Cov and off-state Ig current.

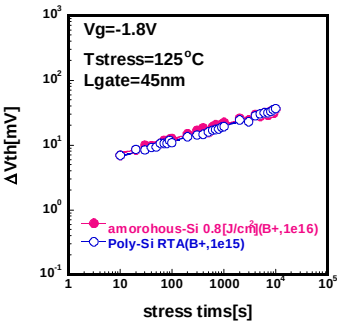


Fig.11. BT stress time dependence of Vth shift for PMOSFETs with LTP and RTA.