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Effects of Base Oxide and Silicon Composition on Charge Trapping in HfSiO/SiO_2 High-k Gate Stacks

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1. Introduction

Threshold voltage instability induced by charge trapping and de-trapping has been extensively studied especially for nMOSFETs with Hf-based high-k gate dielectrics [1-5]. However, charge trapping in HfSiO/SiO_2 dual layer high-k gate stacks has not been studied in detail. This work is to investigate the effects of base oxide and Si composition in HfSiO films on charge trapping in the HfSiO/SiO_2 high–k gate stacks.

2. Experimental

CMOS devices with the polysilicon-gated HfSiO/SiO_2 high-k gate stacks were fabricated using an advanced foundry process technology. Base oxides ranging from 8 to 12 Å were thermally grown, followed by the deposition of MOCVD HfSiO high-k gate dielectrics with 50, 60, and 75% Si composition in the HfSiO films (Si/Hf+Si=50, 60, and 75%) separately to produce an equivalent oxide thickness (EOT) of about 20 Å. In addition, a 19.6-Å oxynitride gate dielectric was also prepared to serve as the control sample.

3. Results and Discussion

Fig. 1 shows the high-resolution Rutherford backscattering spectrometry (RBS) depth profile of the HfSiO/SiO_2 high-k gate stack with 50% Si composition in the HfSiO film (Si/Hf+Si=50%). The carrier transport mechanism of HfSiO/SiO_2 high-k gate stacks under substrate injection condition at various temperatures is shown in Fig. 2. At low field and high temperature, thermally excited electrons hopping from one isolated state to the other yield the ohmic characteristics. At high field and low temperature, however, Frenkel-Poole emission dominates due to field-enhanced thermal excitation of trapped electrons into the conduction band. These results suggest that substantial trap states exist in the HfSiO bulk layer.

Fig. 3 shows the threshold voltage (V_t) shift and the degradation of saturation drain current ($I_{d,sat}$) as a function of stress time for nMOSFETs under various positive gate bias voltages at 125℃. Both V_t shift and $I_{d,sat}$ degradation increased with increasing stress time in two-stage power law relation. Positive gate bias can introduce trapped electrons into the pre-existing HfSiO bulk defects, thus causing the threshold voltage instability [4-5]. Since the maximum transconductance $G_{m,max}$ remains constant during the stress (not shown here), the increase of threshold voltage is mainly responsible for the driving current degradation [1-3]. Fig. 4 shows the linear relation between V_t shift and $I_{d,sat}$ degradation (V_t shift ~ 4.3(mV/%) x $I_{d,sat}$ degradation). The temperature dependence of $I_{d,sat}$ degradation and the two-stage charge trapping process are illustrated in Fig. 5. At the beginning of gate bias stress, channel carriers may be injected into the HfSiO bulk layer by direct tunneling through the base oxide and get trapped in the pre-existing HfSiO bulk traps. Since tunneling emission is essentially independent of temperature, similar charge trapping behaviors are expected at different temperatures. Then these early trapped charges may diffuse along the HfSiO bulk layer, and the diffusion of trapped charges is a thermally activated process with activation energy E_a of about 0.067 eV. Hence severe charge trapping was observed at high temperatures after a prolonged stress. This is the injection-diffusion model.

The effects of base oxide thickness and Si composition in HfSiO films on $I_{d,sat}$ degradation are illustrated in Fig. 6 (a) and (b), respectively. The oxynitride gate dielectric exhibited negligible charge trapping, whereas the extent of charge trapping in the HfSiO/SiO_2 high-k gate stacks increased with the decrease of base oxide thickness and Si composition in HfSiO films. These results can be explained by considering the tunneling time constant across the base oxide and the existence of neutral Hf-OH trapping centers in the HfSiO films. The tunneling time constant increases exponentially with increasing base oxide thickness, and the typical tunneling time constants for 10- and 20-Å base oxides are 0.1 and 100 us, respectively [5]. Moreover, the higher Si composition in HfSiO films means less Hf composition and less neutral Hf-OH trapping centers in the HfSiO bulk layer [2], thus resulting in less charge trapping. Fig. 7 shows that $I_{d,sat}$ degradation increased rapidly in power law relation with the gate bias voltage or the vertical electric field (V_g/EOT). It appears that charge trapping would be less significant under scaled gate bias voltages (<1.2 V) in the future.

4. Conclusion

It is found that ohmic and Frenkel-Poole emission are the major carrier transport mechanisms under substrate injection condition for the HfSiO/SiO_2 high-k gate stacks. The V_t shift induced by charge trapping is mainly responsible for the $I_{d,sat}$ degradation, and there exists a linear

relationship between the V_t shift and $I_{d,sat}$ degradation. Moreover, an injection-diffusion model is proposed to explain the two-stage charge trapping process in the $HfSiO/SiO_2$ high-k gate stacks. Thicker base oxide thickness, higher Si composition in HfSiO films, and lower gate bias voltage are preferred to reduce charge trapping in the $HfSiO/SiO_2$ high-k gate stacks. Nonetheless, more effort is still needed to clarify the physical mechanism in detail.

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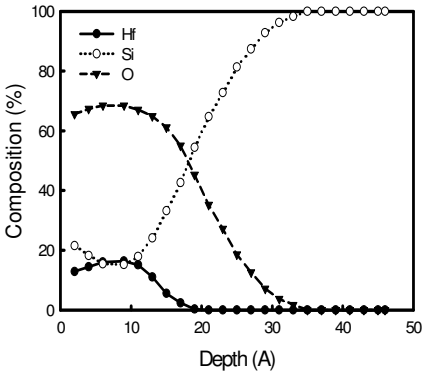

Fig. 1 High-resolution RBS depth profile of $HfSiO(2.0nm)/SiO_2(1.2nm)$ high-k gate stacks.

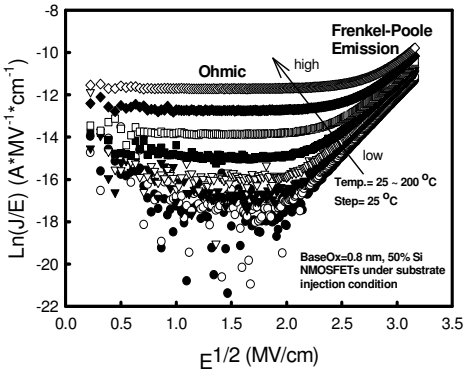

Fig. 2 Carrier transport mechanism of $HfSiO/SiO_2$ high-k gate stacks under substrate injection condition.

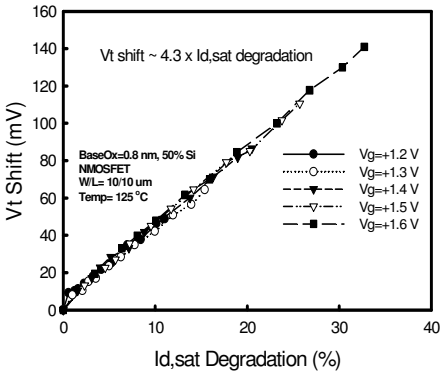

Fig. 4 Linear relation between Vt shift and Id,sat degradation. The increase of Vt is mainly responsible for Id,sat degradation.

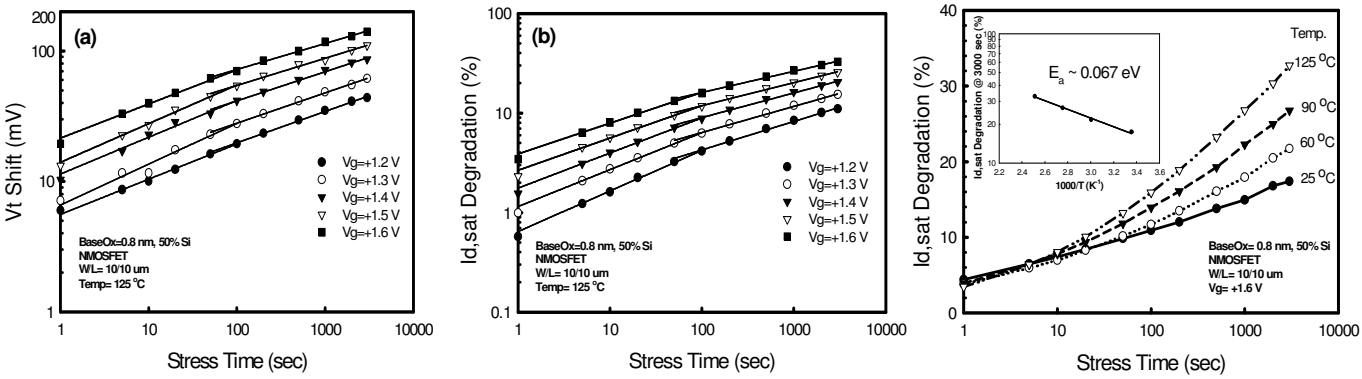

Fig. 3 (a)Vt shift and (b)Id,sat degradation for nMOSFETs under various positive gate bias voltages as a function of stress time. Two-stage power law curve fitting can be observed.

Fig. 5 Temperature dependence of Id,sat degradation. The inset indicates the Ea of trapped charge diffusion is ~ 0.067 eV.

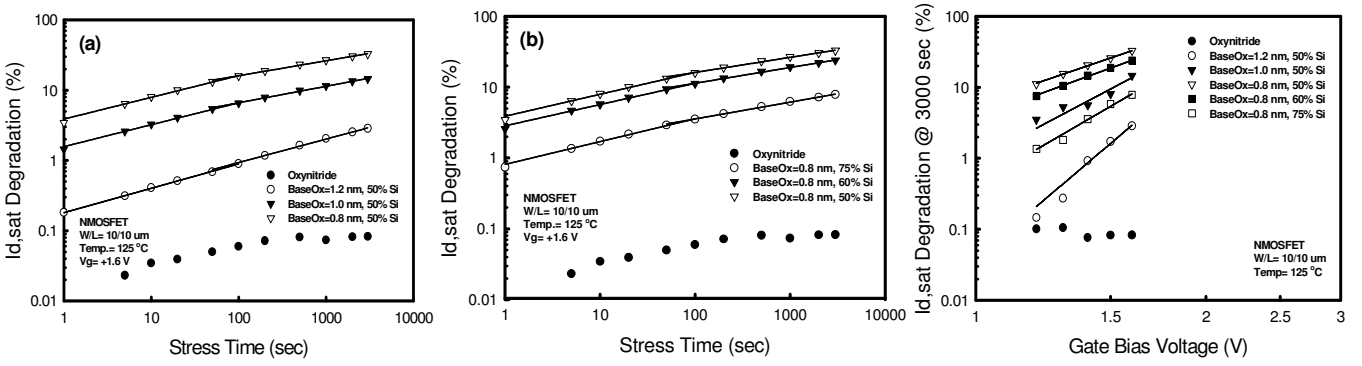

Fig. 6 Effects of (a)base oxide thickness and (b)Si composition in HfSiO films on Id,sat degradation. 1.2-nm base oxide and 75% Si composition are preferred for the reduction of Id,sat degradation.

Fig. 7 Power law dependence of Id,sat degradation on gate bias voltages for various $HfSiO/SiO_2$ high-k gate stacks.