Hysteresis Phenomenon Improvements of HfO₂ by CF₄ Plasma Treatment

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1. Introduction
High-dielectric-constant (high-k) oxide thin films are attracting great interest as replacement for the nitrided-SiO₂ gate oxide film [1-4]. Unfortunately, for HfO₂, there is the hysteresis phenomenon on capacitance voltage (C-V) characteristics. This hysteresis resulted in a flat-band voltage shift, consequently a threshold voltage instability when it is applied to the MOS field-effect transistor as the gate dielectrics. It was reported that the hysteresis phenomenon might be due to chemical contaminations, the stress induced defect formation, or mobile ions [2,5]. Appropriate fluorine incorporation into gate oxide films improved breakdown-distribution tails in Weibull plots, while maintaining both Si/SiO₂ interface characteristics [6]. However, excess fluorine incorporation increased the oxide thickness and degraded not only the reliability of Si/SiO₂ interfaces but also dielectric-breakdown immunity.

In this work, a novel approach was proposed to improve the hysteresis phenomenon. Fluorine was incorporated by CF₄ plasma to improve the characterization of the HfO₂ including leakage current, breakdown voltage and hysteresis phenomenon. An inner-interface trapping model is presented to explain the hysteresis phenomenon.

2. Experiments
MOS capacitors were fabricated on p-Si (100) wafers in this work. Fluorine incorporation into HfO₂ thin films was processing according to the flow as schematic in Fig. 1. HfO₂ is deposited by reactive RF sputter method. Concerning the plasma damages, the CF₄ plasma was performed directly on HfO₂ thin films for 1, 3, and 5 min at 300 °C under the low power of 50 watts. Fluorine diffuses through HfO₂ thin film and accumulated at the underlying interfacial regions as shown in Fig. 2. Aluminum was evaporated for top and bottom electrode. The electrical properties were analyzed by HP 4285 precision LCR meters for capacitance-voltage (C-V) characteristics, and HP4156 for current-voltage (I-V) F-N curves. The fluorine and silicon concentration was measured by secondary ion mass spectroscopy (SIMS).

3. Results and Discussion

Physical and Electrical Characterization
A typical fluorine profile measured by using secondary ion mass spectroscopy (SIMS) is shown in Fig. 3. It is clarified that fluorine atoms were accumulated mainly at the HfO₂/silicon substrate interface. The I-V curves were shown in Fig. 4 for all samples. The gate leakage current decreased with increasing CF₄ plasma treatment when the CF₄ plasma time is lower than 3 minutes. However, the gate leakage current increased much for the sample with 5 minutes CF₄ plasma treatment. The same tendency for breakdown voltage behavior and distribution was shown in Fig. 5. The C-V curve was shown in Fig. 6 where the inset shows the CF₄ plasma treatment effects on EOT. The plasma treatment condenses the HfO₂ and results in higher capacitances. Wright et al. proposed that fluorine atoms react with Si-O bonds, and released oxygen atoms to increase the SiO₂ thickness [7]. Fortunately, there’s no thickness increasing by the fluorine incorporation into the HfO₂ interfaces.

Hysteresis of C-V Characteristics
The hysteresis of C-V characteristics were shown in Fig. 7 (a), (b), (c) and (d) for control, CF₄ plasma treatment 1, 3 and 5 min, respectively. The C-V characteristics for hysteresis were measuring the curve by sweeping the voltage from accumulation to inversion and then sweeping back (-3V→0V→-3V). A shift of about 1.2 V is observed for control sample. The hysteresis phenomenon was much improved after CF₄ plasma treatment. A shift was reduced to 40 mV for samples with CF₄ plasma treatment.

Mechanism of Hysteresis for HfO₂
The mechanism of hysteresis is shown in Fig. 8 and Fig. 9 for control and sample with CF₄ plasma treatment, respectively. When the capacitor is first at accumulation (Vₘₐₓ=-3.0 V), majority carriers (holes for the p-type Si substrate) tunnel from p-Si substrate through the Hf-silicate layer and are trapped at the inner-interface, as shown in Fig. 8(a). When the voltage is swept toward the positive direction, the C-V curve shifts negatively. Then, when the voltage is swept to the positive side to make the capacitor stay at inversion (Vₘₐₓ=0 V), the trapped holes at the inner-interface will be de-trapped and at the same time. Minority carriers (electrons) will tunnel from the p-Si substrate and trapped at the inner-interface, as shown in Fig. 8(b). This makes the C-V curve shift positively when the voltage is swept toward the negative side. The mechanism makes the C-V curve have a hysteresis loop. After CF₄ plasma treatment, the trapping effects can be reduced. It’s consistent with the breakdown voltage improvement. The fluorine incorporation strengthen the interface quality and resulted in less hysteresis as shown in Fig. 9.

4. Conclusion
A novel approach to improve the hysteresis of the HfO₂ by CF₄ plasma treatment was proposed. Appropriate fluorine ions incorporation into Hf-silicate improved the characterization including gate leakage current and hysteresis. An inner-interface traps model can explain the hysteresis of C-V characteristics before and after CF₄ plasma treatment.

References
Fig.1. The key processes in this work for (a) sample with CF$_4$ plasma treatment and (b) control sample without CF$_4$ plasma, respectively.

Fig.2. Physical model for post-CF$_4$ plasma treatment was schematic. The fluorine was incorporated into Hf-silicate after CF$_4$ plasma treatment.

Fig.3. The SIMS depth profile of MOS structure for fluorine. The peak position is the interface of HfO$_2$ and silicon substrate.

Fig.4. The J-V curves (gate leakage current) for all sample. The leakage current was reduced for sample with CF$_4$ plasma treatment 1 and 3 min.

Fig.5. The Weibull plots for different CF$_4$ plasma treatment. The inset figure is the relationship between EOT and plasma time.

Fig.6. The C-V curves for different CF$_4$ plasma treatment. The inset figures are the relationship between EOT and plasma time.

Fig.7. The hysteresis of C-V characteristics for sample (a) without CF$_4$ plasma treatment (b) with CF$_4$ plasma treatment 1 min (c) with CF$_4$ plasma treatment 3 min (d) with CF$_4$ plasma treatment 5 min, respectively.

Fig.8. (a) Inner-interface trapping model of the hafnium dielectrics sweeping from inversion ($V_g = 0$ V). (b) Inner-interface trapping model of the hafnium dielectrics sweeping from accumulation ($V_g = -3.0$ V).

Fig.9. (a) Inner-interface trapping model of the hafnium dielectrics sweeping from inversion after CF$_4$ plasma treatment. (b) Inner-interface trapping model of the hafnium dielectrics sweeping from accumulation after CF$_4$ plasma treatment ($V_g = -3.0$ V).