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Hysteresis Phenomenon Improvements of HfO_2 by CF_4 Plasma Treatment

Chao Sung Lai[1], Woei Cherng Wu[2], Kung Ming Fan[3], Jer Chyi Wang[4], and Shian-Jyh Lin[5]
[1,2,3] Department of Electronic Engineering, Chang Gung University,
[4,5] Nanya Technology Corp., Technology Process Development Department, Tao-Yuan, Taiwan
259 Wen-Hwa 1st Road, Kwei-Shan, Tao-Yuan, Taiwan
Phone: +886-3-2118800 ext 5786 E-mail: cslai@mail.cgu.edu.tw

1. Introduction

High-dielectric-constant (high-*k*) oxide thin films are attracting great interest as replacement for the nitrided-SiO_2 gate oxide film [1-4]. Unfortunately, for HfO_2, there is the hysteresis phenomenon on capacitance voltage (C-V) characteristics. This hysteresis resulted in a flat-band voltage shift, consequently a threshold voltage instability when it is applied to the MOS field-effect transistor as the gate dielectrics. It was reported that the hysteresis phenomenon might be due to chemical contaminations, the stress induced defect formation, or mobile ions [2,5]. Appropriate fluorine incorporation into gate oxide films improved breakdown-distribution tails in Weibull plots, while maintaining both Si/SiO2 interface characteristics [6]. However, excess fluorine incorporation increased the oxide thickness and degraded not only the reliability of Si/SiO2 interfaces but also dielectric-breakdown immunity.

In this work, a novel approach was proposed to improve the hysteresis phenomenon. Fluorine was incorporated by CF_4 plasma to improve the characterization of the HfO_2 including leakage current, breakdown voltage and hysteresis phenomenon. An inner-interface trapping model is presented to explain the hysteresis phenomenon.

2. Experiments

MOS capacitors were fabricated on p-Si (100) wafers in this work. Fluorine incorporation into HfO_2 thin films was processing according to the flow as schematic in Fig. 1. HfO_2 is deposited by reactive RF sputter method. Concerning the plasma damages, the CF_4 plasma was performed directly on HfO_2 thin films for 1, 3, and 5 min at 300 °C under the low power of 50 watts. Fluorine diffuses through HfO_2 thin film and accumulated at the underlying interfacial regions as shown in Fig 2. Aluminum was evaporated for top and bottom electrode. The electrical properties were analyzed by HP 4285 precision LCR meters for capacitance-voltage (C-V) characteristics, and HP4156 for current-voltage (I-V) F-N curves. The fluorine and silicon concentration was measured by secondary ion mass spectroscopy (SIMS).

3. Results and Discussion

Physical and Electrical Characterization

A typical fluorine profile measured by using secondary ion mass spectroscopy (SIMS) is shown in Fig. 3. It is clarified that fluorine atoms were accumulated mainly at the HfO_2/silicon substrate interface. The I-V curves were shown in Fig. 4 for all samples. The gate leakage current decreased with increasing CF_4 plasma treatment when the CF_4 plasma time is lower than 3 minutes. However, the gate leakage current increased much for the sample with 5 minutes CF_4 plasma treatment. The same tendency for breakdown voltage behavior and distribution was shown in Fig. 5. The C-V curve was shown in Fig. 6 where the inset shows the CF_4 plasma treatment effects on EOT. The plasma treatment condenses the HfO_2 and results in higher capacitances. Wright *et al.* proposed that fluorine atoms react with Si-O bonds, and released oxygen atoms to increase the SiO_2 thickness [7]. Fortunately, there's no thickness increasing by the fluorine incorporation into the HfO_2 interfaces.

Heysteresis of C-V Characteristics

The heysteresis of C-V characteristics were shown in Fig. 7 (a), (b), (c) and (d) for control, CF_4 plasma treatment 1, 3 and 5 min, respectively. The *C–V* characteristics for heysteresis were measuring the curve by sweeping the voltage from accumulation to inversion and then sweeping back (-3V→ 0V→-3V). A shift of about 1.2 V is observed for control sample. The heysteresis phenomenon was much improved after CF_4 plasma treatment. A shift was reduced to 40 mV for samples with CF_4 plasma treatment..

Mechanism of Heysteresis for HfO_2

The mechanism of heysteresis is shown in Fig. 8 and Fig. 9 for control and sample with CF_4 plasma treatment, respectively. When the capacitor is first at accumulation (Vg=-3.0 V), majority carriers (holes for the *p*-type Si substrate) tunnel from *p*-Si substrate through the Hf-silicate layer and are trapped at the inner-interface, as shown in Fig. 8(a). When the voltage is swept toward the positive direction, the *C–V* curve shifts negatively. Then, when the voltage is swept to the positive side to make the capacitor stay at inversion (Vg=0 V), the trapped holes at the inner-interface will be de-trapped and at the same time. Minority carriers (electrons) will tunnel from the *p*-Si substrate and trapped at the inner-interface, as shown in Fig. 8(b). This makes the *C–V* curve shift positively when the voltage is swept toward the negative side. The mechanism makes the *C–V* curve have a hysteresis loop. After CF_4 plasma treatment, the trapping effects can be reduced. It's consistent with the breakdown voltage improvement. The fluorine incorporation strengthen the interface quality and resulted in less heysteresis as shown in Fig. 9.

4. Conclusion

A novel approach to improve the heysteresis of the HfO_2 by CF_4 plasma treatment was proposed. Appropriate fluorine ions incorporation into Hf-silicate improved the characterization including gate leakage current and heysteresis. An inner-interface traps model can explain the heysteresis of C-V characteristics before and after CF_4 plasma treatment.

References

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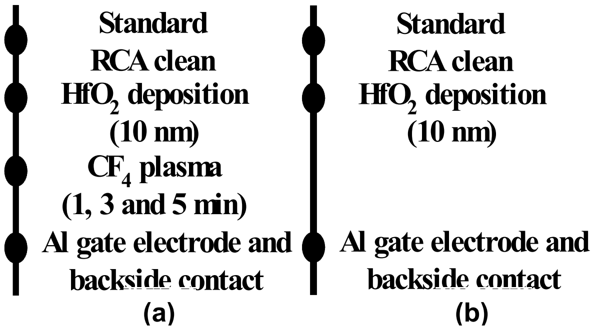

Fig.1. The key processes in this work for (a) sample with CF_4 plasma treatment and (b) control sample without CF_4 plasma), respectively.

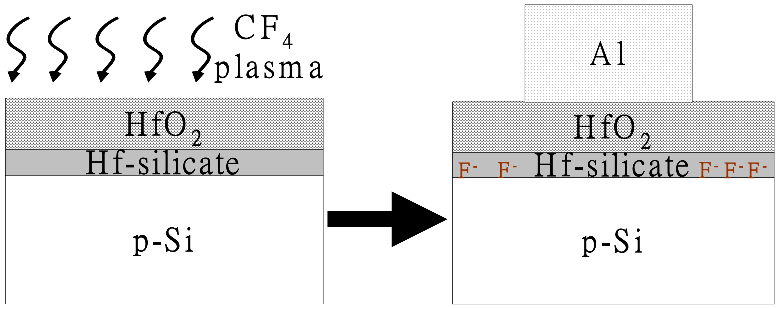

Fig.2. Physical model for post-CF_4 plasma treatment was schematic. The fluorine was incorporated into Hf-silicate after CF_4 plasma treatment.

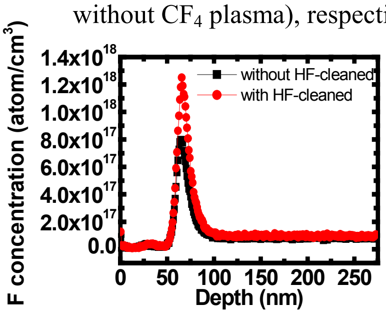

Fig.3. The SIMS depth profile of MOS structure for fluorine. The peak position is the interface of HfO_2 and silicon substrate.

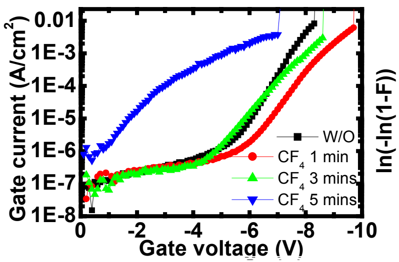

Fig.4. The J-V curves (gate leakage current) for all sample. The leakage current was reduced for sample with CF_4 plasma treatment 1 and 3 min

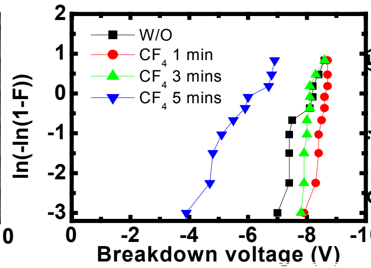

Fig.5. The Weibull plots for different CF_4 plasma treatment. The breakdown voltage was increased for sample with CF_4 plasma treatment 1 and 3 min

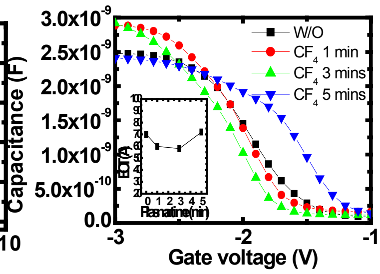

Fig.6. The C-V curves for different CF_4 plasma treatment. The inset figure is the relationship between EOT and plasma time.

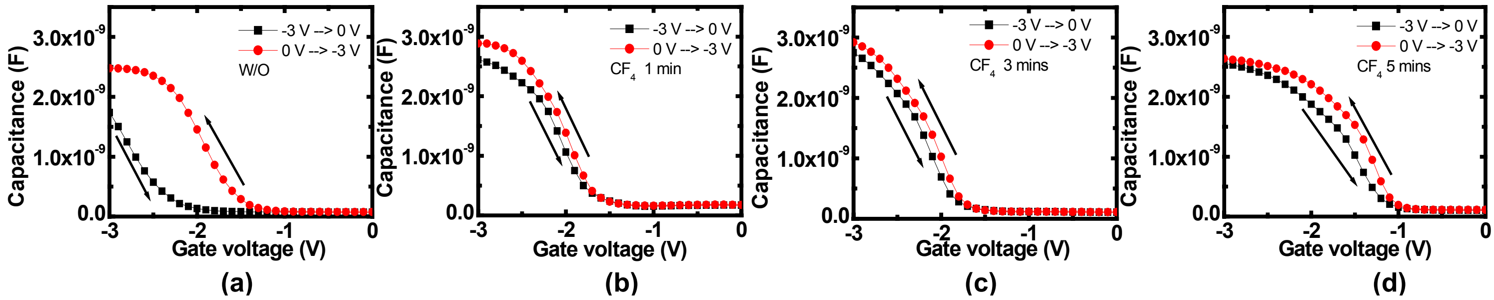

Fig.7. The hysteresis of C-V characteristics for sample (a) without CF_4 plasma treatment (b) with CF_4 plasma treatment 1 min (c) with CF_4 plasma treatment 3 min (d) with CF_4 plasma treatment 5 min, respectively.

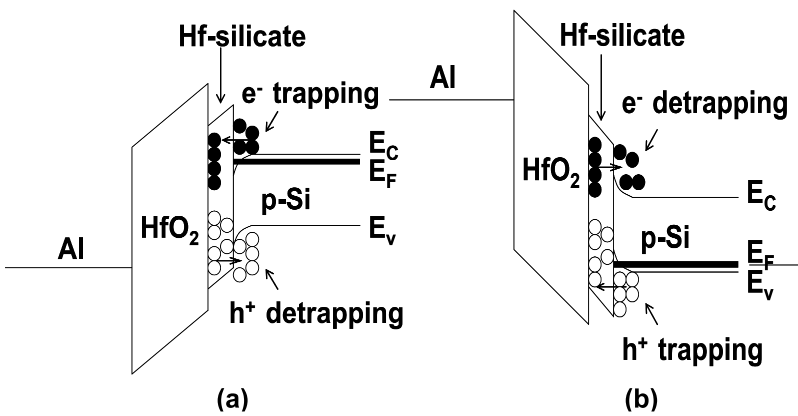

Fig.8. (a) Inner-interface trapping model of the hafnium dielectrics sweeping from inversion (Vg = 0 V). (b) Inner-interface trapping model of the hafnium dielectrics sweeping from accumulation (Vg = -3.0 V).

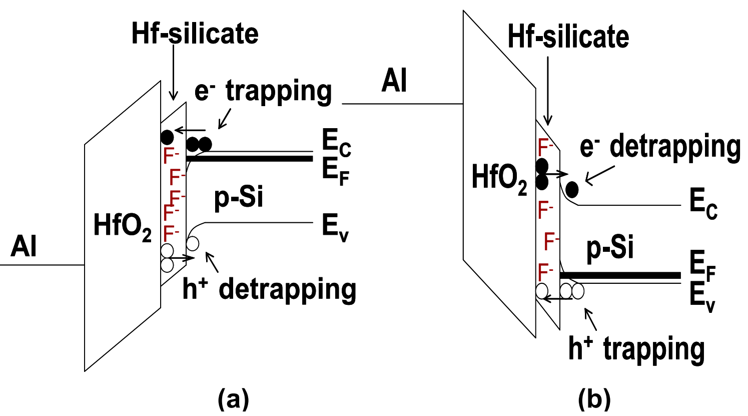

Fig.9. (a) Inner-interface trapping model of the hafnium dielectrics sweeping from inversion (Vg = 0 V) after CF_4 plasma treatment. (b) Inner-interface trapping model of the hafnium dielectrics sweeping from accumulation after CF_4 plasma treatment (Vg = -3.0 V).