Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 744-745

B-7-3

Effects of post-deposition anneal on the electrical properties in HfSiO films grown by atomic layer deposition

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1. Introduction

HfSiO has recently proven to be a promising high-k dielectric with lower diffusivity of impurities and improved channel mobility characteristics [1]. However, it was demonstrated that under a high temperature anneal, HfSiO tended to separate into the individual phases (SiO_2 and metal oxide) [2]. The concerns for crystallization as well as the phase separation have led to the modification of these silicate films by adding nitrogen [2]. In this study, post-deposition annealing (PDA) gas of NH_3 was used to incorporate nitrogen in HfSiO film deposited by atomic layer deposition (ALD). The effects of NH_3 anneal on electrical properties of ALD HfSiO MOSFETs were compared with the case of N_2 anneal.

2. Experimental

Self-aligned MOSFETs with poly-Si gates were fabricated via process steps shown in Table 1. LPCVD silane poly-Si was deposited at 620°C and implanted with phosporous and BF_2 for N- and P-MOSFETs, respectively. RTA activation was done at 1000°C for 10 sec in N_2. HfSiO gate dielectric with Hf/Si=1/1 ratio by XPS was deposited by ALD using an oxidized gas of O_3. Post-deposition anneal was performed in N_2 at 950°C for densification or in NH_3 at 750°C for incorporating nitrogen in the film.

3. Results and Discussion

The growth rates of ALD HfSiO and SiO_2 films as a function of substrate temperature are shown in Fig. 1. As substrate temperature increases from 250°C to 350°C, the growth rate of HfSiO increases due to the enhanced growth rate of ALD-SiO_2. The interface thickness is measured from TEM image in Fig. 2, where the interface between HfSiO film and Si substrate is about 13A. This thick interfacial layer is assumed to be due to the high flow rate of oxidizing gas at the initial step of ALD process. Fig. 3 shows C-V characteristics of 30Å-thick HfSiO MOS transistors in accumulation region with post-deposition anneal using NH_3 gas at 750°C. The negligible hysteresis in Fig. 3 indicates that the contribution of high-k portion to hysteresis is reduced by the thick interface. As described in Fig. 4, the NH_3 anneal shifted threshold voltage (Vth) of HfSiO MOS transistors without PDA by about 100mV, which is due to the positive fixed charge induced during the anneal. In addition, slightly higher reverse short channel effects than SiO_2 cases are detected in both NMOS and PMOS transistors. Fig. 5 shows Vfb and hysteresis of HfSiO films with various thicknesses. The Vfb is found to be independent of the film thickness. On the other hand, the hysteresis increases with increasing film thickness, which implies that pre-existing trap density is larger in thicker film. Fig. 6 shows the comparison of stress induced leakage currents (SILCs) of NH_3 annealed HfSiO films with different thickness, where the insignificant SILC is observed, independent of film thickness. These SILC and hysteresis behavior are also observed in the same way in the HfSiO films without PDA. Normalized Id's with respect to EOT from NMOSFETs are compared in Fig. 7. It is found that thicker film with NH_3 anneal degrades the Idsat more than thinner film with NH_3 anneal, which is consistent with hysteresis behavior. In contrast, the hysteresis found in thicker HfSiO film with NH_3 anneal disappears in the HfSiO film with N_2 anneal as shown in Fig. 8. This indicates that PDA with N_2 reduces the trap density resulting in negligible hysteresis. Furthermore, the N_2 anneal in Fig. 9 reduced SILC, indicating the densification of the film. The mobility of three films with different PDA is compared in Fig. 10. NH_3 anneal does not degrade the mobility of HfSiO films, which is possibly due to the thick interfacial layer. However, N_2 anneal improves the mobility by about 15%, which results in enhanced Idsat from N_2 annealed HfSiO devices as shown as shown in Fig. 11. Therefore, the combination of NH_3 anneal and N_2 anneal is desirable to achieve higher dielectric constant with nitrogen incorporation as well as minimized hysteresis compared to as-deposited film.

4. Conclusion

HfSiO films with thick interfacial layer were deposited by ALD. Poly-gated MOSFETs showed negligible hysteresis in 30Å thick HfSiO films while increasing in the thicker films. Although NH_3 anneal did not degrade film quality while increasing dielectric constant, it did not cure the hysteresis problem in thicker film. In addition, it was found that N_2 anneal was effective method for reducing the hysteresis. Therefore, the combination of NH_3 anneal and N_2 anneal was required to increase dielectric constant and to enhance densification, respectively.

References

1. A. Morioka et al., Symp. VLSI Tech., p. 65, 2003.
2. M. Koyama et al., IEDM Tech. Dig., p. 849, 2002.

- Field oxidation & Active patterning
- Vt adjust implant
- 100:1HF clean
- ALD HfSiO deposition
- Post-deposition anneal
- Poly-Si deposition
- Gate patterning (RIE)
- S/D implant
- S/D activation : 1000℃, 10sec
- Co-salicide
- Metallization
- FG anneal

Table.1 Process flow for HfSiO MOSFETs.

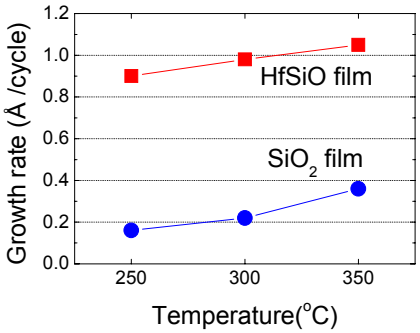

Fig.1 HfSiO and SiO_2 films are grown faster with higher substrate temperatures by ALD process.

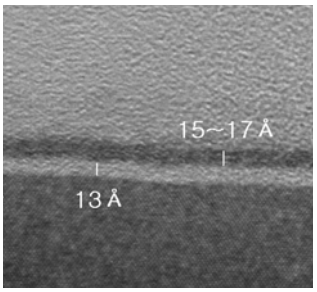

Fig.2 The thickness of Interface layer between ALD HfSiO and Si substrate is found to be about 13 Å .

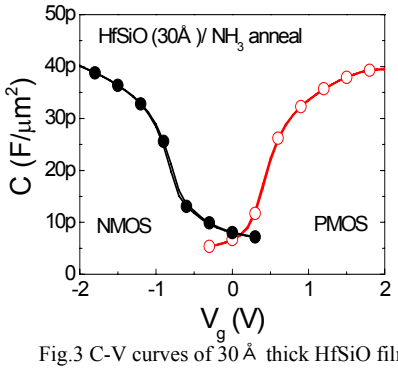

Fig.3 C-V curves of 30 Å thick HfSiO films with NH_3 post-anneal.

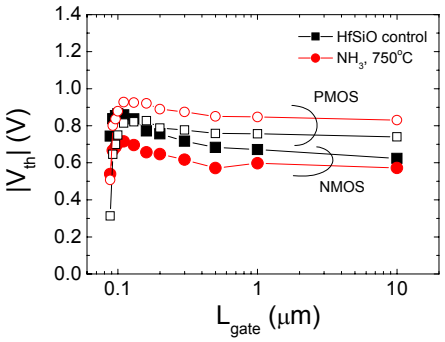

Fig.4 Nitridation of 30 Å -thick HfSiO films with NH_3 anneal affects MOSFET Vth by about 0.1V.

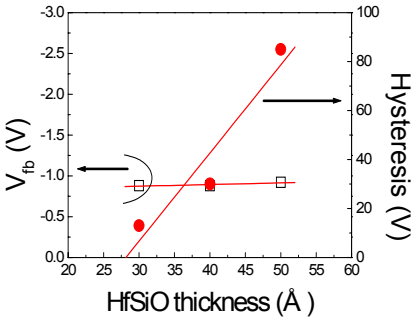

Fig.5 Nitrided HfSiO film by NH_3 anneal shows higher hysteresis as film thickness increases.

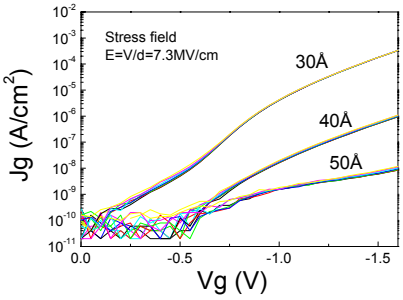

Fig.6 Stressed induced leakage current (SILC) is independent of HfSiO film thickness.

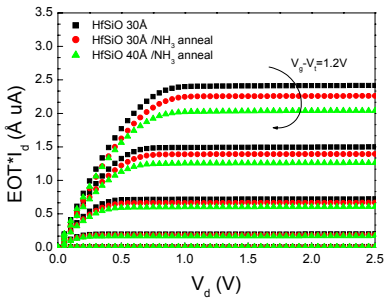

Fig.7 Idsat is worse in NH_3 annealed and thicker HfSiO films.

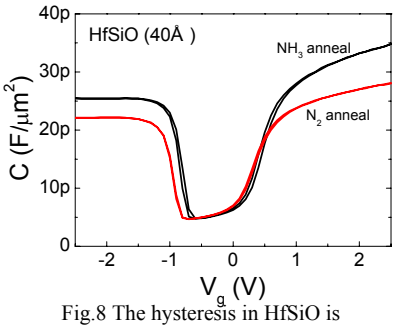

Fig.8 The hysteresis in HfSiO is prevented by post-N_2 anneal.

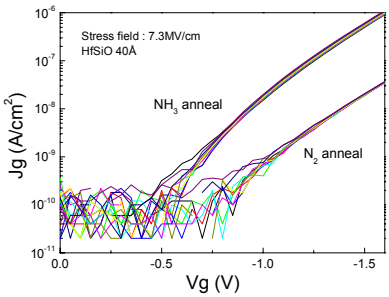

Fig.9 Stressed induced leakage current of HfSiO film is reduced by post-N_2 anneal.

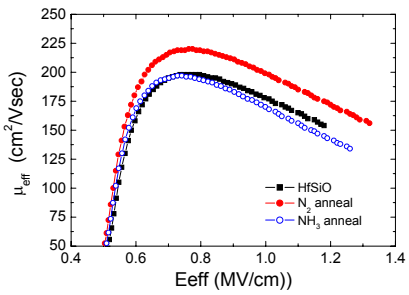

Fig.10 Comparison of channel mobility of HfSiO with and without N_2 or NH_3 anneal in NMOSFETs.

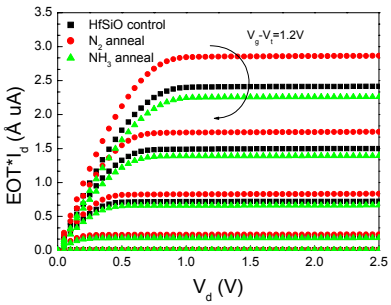

Fig.11 Idsat is enhanced by N_2 anneal of HfSiO films.