

# High Performance fully silicided NiSi:Hf gate on LaAlO<sub>3</sub>/GOI n-MOSFET with Little Fermi-level Pinning

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## 1. Introduction

The main challenges for metal-gate/high- $\kappa$  CMOS are the Fermi-level pinning and mobility degradation. The Fermi-level pinning shifts the original low or high workfunction to midgap that causes the intolerable  $|V_T|$  increase. The possible mechanism of Fermi-level pinning is due to the interface reaction and dipole creation of high- $\kappa$  dielectric with poly-Si or metal-nitride at high RTA temperatures. In this paper, we have successfully developed the 4.2 eV low workfunction fully silicided NiSi:Hf gate on novel high- $\kappa$  LaAlO<sub>3</sub>/Ge-on-Insulator (GOI) [1]-[2] n-MOSFETs. The fully silicided gate has special virtue of simple process compatible to current VLSI [1]. Little Fermi-level pinning is evidenced from the nearly identical workfunction of NiSi:Hf on SiO<sub>2</sub>/Si and LaAlO<sub>3</sub>/GOI MOSFETs, which may be due to the low temperature 500°C RTA process and robust LaAlO<sub>3</sub> dielectric. The achieved low workfunction is close to ideal value from poly-Si gate, which is due to the added Hf to lower down workfunction of NiSi (4.55 eV). The high- $\kappa$  LaAlO<sub>3</sub> has unique merits of free from moisture degradation unlike La<sub>2</sub>O<sub>3</sub>, preserving high- $\kappa$  (~25) near La<sub>2</sub>O<sub>3</sub> [3]-[4] by adding Al<sub>2</sub>O<sub>3</sub> [1]-[2], and widely available for superconductor application. This is in sharp contrast to HfAlO<sub>x</sub> with largely lowered  $\kappa$  from HfO<sub>2</sub> for improving thermal stability. The high performance NiSi:Hf/LaAlO<sub>3</sub>/GOI n-MOSFETs is evidenced from the ~5 orders of magnitude lower leakage current at 1.4 nm EOT and high electron mobility of 398 cm<sup>2</sup>/Vs (1.7X higher than LaAlO<sub>3</sub>/Si). The poly-Si comparable workfunction, little Fermi-level pinning, low leakage current, high mobility, low thermal budget and process compatible to current VLSI are the merits for NiSi:Hf/LaAlO<sub>3</sub>/GOI MOSFETs.

## 2. Experimental

We have used the proton implantation and smart cut to form the thin top layer GOI [1]-[2]. After transistor active region definition, the n<sup>+</sup> source and drain were implanted by Phosphorus to GOI or Si and followed by 500°C or 950°C annealing, respectively. The high- $\kappa$  LaAlO<sub>3</sub> gate dielectric was deposited from a LaAlO<sub>3</sub> source ( $\kappa$ =25.1) followed by 400°C oxidation and annealing. Then amorphous Si was deposited on LaAlO<sub>3</sub>. The fully silicided NiSi:Hf gate was formed by depositing Hf and driven-in by 1<sup>st</sup> RTA, and Ni deposition to form the NiSi:Hf gate by 2<sup>nd</sup> RTA. For comparison, the Al gate devices and SiO<sub>2</sub> gate dielectric devices are also formed.

## 3. Results and Discussion

To study the workfunction pinning, we have first measured the workfunction of NiSi:Hf on SiO<sub>2</sub>/Si MOSFET. Fig. 1 shows the SiO<sub>2</sub> thickness-dependent  $V_{FB}$  plot. A workfunction of 4.3 eV is obtained for NiSi:Hf and lower than NiSi (4.55 eV) due to the interface Hf. Note that the 4.3 eV is very close to poly-Si gate n-MOS. Because Hf cannot form low resistivity silicide at 500°C RTA, the 2<sup>nd</sup> RTA formed NiSi, with interface workfunction control Hf, is crucial for achieving low resistivity of 45  $\mu\Omega$ -cm fully silicided gate. Such resistivity is close to that of NiSi. To the best of our knowledge, this is the first report to achieve both low workfunction and low resistivity simultaneously in fully silicided gate.

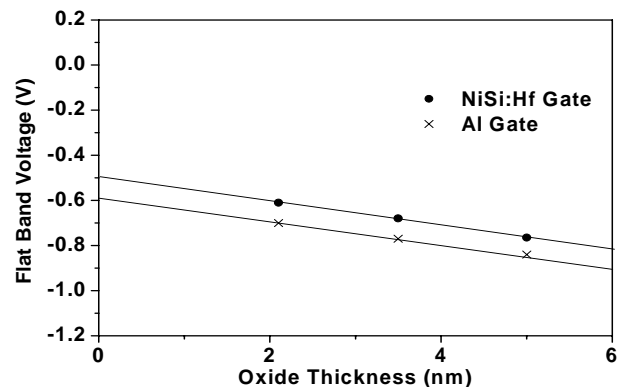


Fig. 1. The  $V_{fb}$  versus SiO<sub>2</sub>-thickness plot of n-MOS capacitors with fully NiSi:Hf and Al gates.

Fig. 2 shows the measured C-V characteristics. The same inversion and accumulation capacitance using fully silicided NiSi:Hf suggests no gate depletion. The small  $V_{fb}$  shift is due to slight increase of work function. An EOT of 1.4 nm is obtained that gives a  $\kappa$  value of 22.6 at the 8.1 nm thick LaAlO<sub>3</sub> on Si from X-TEM. From the measured  $V_{fb}$ , workfunction of 4.2-4.3 eV is obtained for NiSi:Hf on SiO<sub>2</sub> or LaAlO<sub>3</sub> and summarized in Table 1 that indicating little Fermi-level pinning.

Fig. 3 is the gate dielectric J-V characteristics plotted at  $V_g - V_{fb}$ . The leakage current is ~5 orders of magnitude lower in LaAlO<sub>3</sub> than SiO<sub>2</sub> at 1.4 nm EOT due to the thick high- $\kappa$  of LaAlO<sub>3</sub>. The lower leakage current in NiSi:Hf gate device is due to slightly higher workfunction than Al.

Fig. 4 shows the  $I_d - V_d$  characteristics. The near identical  $I_d - V_d$  plotted at same  $V_g - V_t$  of NiSi:Hf with Al control devices suggests no degradation of n-MOSFETs.

The  $I_d$  is significant higher using GOI than Si. The calculated workfunction from measured  $V_t$  of NiSi:Hf on  $\text{SiO}_2/\text{Si}$ ,  $\text{LaAlO}_3/\text{Si}$  and  $\text{LaAlO}_3/\text{GOI}$  devices is shown in Table 1 with almost the same value of  $\sim 4.2\text{--}4.3$  eV. The close workfunction and small  $V_t$  also suggest little Fermi-level pinning, since  $V_t = V_{fb} + 2\phi_B + \sqrt{(4q\epsilon_s N_a \phi_B)/C_{ox}}$ .

Fig. 5 is the electron mobility of  $\text{LaAlO}_3/\text{Si}$  and  $\text{LaAlO}_3/\text{GOI}$  n-MOSFETs. The electron mobility for Al and NiSi:Hf on  $\text{LaAlO}_3/\text{Si}$  MOSFETs has high  $235\text{ cm}^2/\text{Vs}$  value and comparable to metal-gate/HfO<sub>2</sub>. The mobility further increases by 1.7X to  $398\text{ cm}^2/\text{Vs}$  using GOI. In combining with GOI p-MOS data [1]–[2], both hole and electron mobility can be largely improved in GOI.

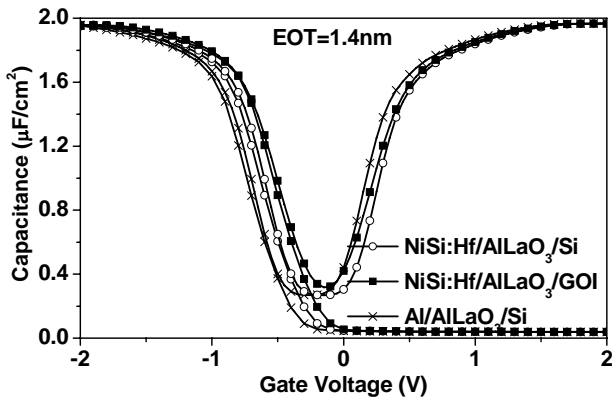


Fig. 2. The measured C-V characteristics  $\text{LaAlO}_3/\text{Si}$  and  $\text{LaAlO}_3/\text{GOI}$  n-MOSFETs with fully silicided NiSi:Hf gate and Al control gate.

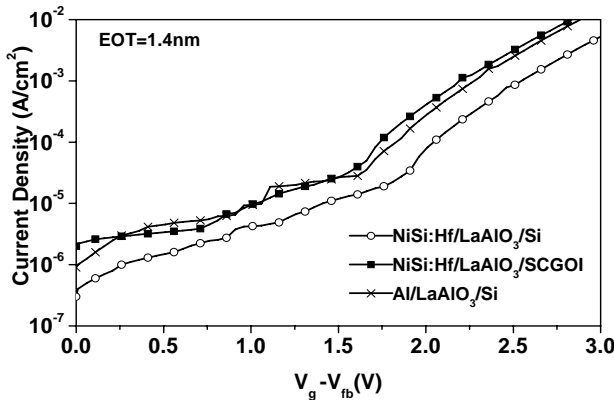


Fig. 3. The measured J-V characteristics of  $\text{LaAlO}_3/\text{Si}$  and  $\text{LaAlO}_3/\text{GOI}$  n-MOSFETs with NiSi:Hf and Al gates.

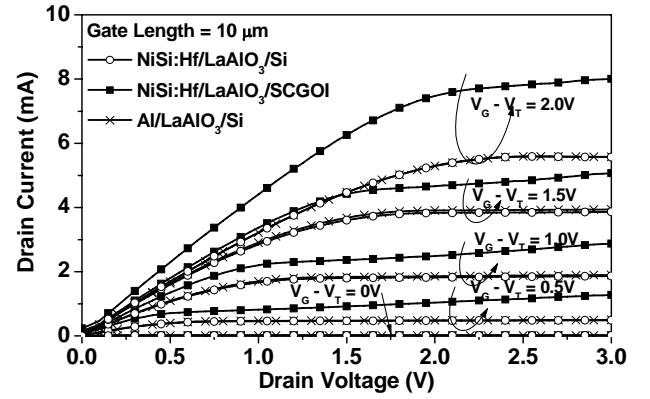


Fig. 4. The  $I_d$ - $V_d$  characteristics of  $\text{LaAlO}_3/\text{Si}$  and  $\text{LaAlO}_3/\text{GOI}$  n-MOSFETs with NiSi:Hf and Al gates.

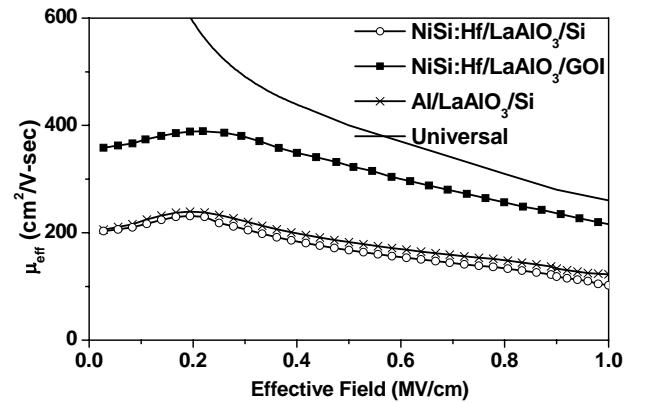


Fig. 5. The electron mobility of  $\text{LaAlO}_3/\text{Si}$  and  $\text{LaAlO}_3/\text{GOI}$  n-MOSFETs with NiSi:Hf and Al gates.

#### 4. Conclusion

We have demonstrated low workfunction, low resistivity, and high performance NiSi:Hf gate on  $\text{LaAlO}_3/\text{GOI}$  n-MOSFETs. These GOI devices have unique merits of dislocation free property for high yield, little Fermi-level pinning, high both electron and hole mobility, no high- $\kappa$  crystallization, little interface reaction or EOT reduction and fully process compatible to current VLSI technology.

#### References

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Table 1. The device parameters for NiSi:Hf/ $\text{SiO}_2/\text{Si}$  (1.9 nm EOT), NiSi:Hf/ $\text{LaAlO}_3/\text{Si}$  (1.4 nm EOT) and NiSi:Hf/ $\text{LaAlO}_3/\text{GOI}$  (1.4 nm EOT) MOSFETs, where  $V_{fb} = (\Phi_m - \Phi_s) - Q_{ox}/C_{ox}$ ;  $\Phi_s = X' + E_g/2e + \phi_B$ .

	$V_{fb}$ (V)	$X'$ (eV)	$E_g$ (eV)	$N_a$ ( $\text{cm}^{-3}$ )	$\phi_B$ (V)	$Q_{ox}$ ( $\#/\text{cm}^2$ )	$C_{ox}$ ( $\mu\text{F}/\text{cm}^2$ )	$\Phi_{mCV}$ (V)
NiSi:Hf/ $\text{SiO}_2/\text{Si}$	-0.58	4.05	1.12	$1 \times 10^{15}$	0.30	$1 \times 10^{11}$	$1.56 \times 10^{-6}$	4.26
NiSi:Hf/ $\text{LaAlO}_3/\text{Si}$	-0.47	4.05	1.12	$1 \times 10^{15}$	0.30	$-2 \times 10^{12}$	$1.92 \times 10^{-6}$	4.29
NiSi:Hf/ $\text{LaAlO}_3/\text{GOI}$	-0.13	4.0	0.66	$5 \times 10^{16}$	0.20	$-2 \times 10^{12}$	$1.92 \times 10^{-6}$	4.23