Effects of high pressure hydrogen and deuterium annealing on nMOSFET with Hf-base gate dielectrics

Hokyung Park, Byoungjun Lee*, Mark Gardner**, and Hyunsang Hwang

Department of Materials Science and Engineering, Gwangju Institute of Science and Technology,
#1, Oryong-dong, Buk-gu, Gwangju 500-712, KOREA
International SEMATECH, *IBM Assignee, **AMD assignee, 2706 Montopolis Drive, Austin, Texas, U.S.A.
Phone: +82-62-970-2314, Fax: +82-62-970-2304, e-mail: hwanghs@gist.ac.kr

Introduction
Mobility degradation of high-k MOSFET is one of the major concern for aggressively scaled CMOSFET technologies. In general, carrier mobility of n-channel high-k MOSFET is more severely degraded than that of p-channel device.[1] It can be explained by high interface trap density in the upper half of the band-gap, which preferential affects n-channel MOSFET.[2]

It is well known that forming gas anneal at 400-450°C is sufficient to completely passivate the interface state of SiO2 gate dielectric. However, conventional forming gas annealing at 400-450°C is not sufficient for high-k gate dielectric.[3-4] Recently we reported improved interface characteristics of HfO2 MIS capacitors by employing high pressure anneal.[5]

In this paper, we have investigated, the effect of high pressure pure (100%) hydrogen annealing on electrical and reliability characteristics of high-k nMOSFET.

Experimental
After standard cleaning of silicon wafer followed by HF-last treatment, nitridation was performed in N2H4 ambient at 700°C. Then, Hf-silicate (2nm) and HfAlO (2nm) layers are deposited in sequence and the stacked high-k layer is annealed in N2 ambient at 700°C. Then, 10nm MOCVD TiN layer and 180nm amorphous silicon layer are deposited as a stack electrode. After the gate patterning, high-k layer is removed with a wet etch process leaving a minimal damage in the extension region. Then, LDD and halo dopants are implanted and a thin nitride layer (~5nm) is deposited to prevent the process induced damage through plasma process or oxygen diffusion. After the thin nitride deposition, 100nm oxide spacer is formed and source/drain is implanted with As and B and activated using 1000°C, 10sec RTA in N2 ambient. After the Ti silicide formation, 700nm pre-metal dielectric (PMD) layer is formed. Then, W plug with Ti/TiN liner is used to contact the S/D and gate electrode regions and Al metal pad is patterned. Conventional forming gas (H2/Ar=4%/96%) annealing was performed at 480°C for 30 minutes, followed by various high pressure annealing in pure (100%) hydrogen ambient for 30min at 400°C. The process sequence is summarized as shown in table 1.

Results & Discussion
Drain current (I(D)) and transconductance (g_(m,na)) vs. gate voltage (V_G) characteristics of nMOSFET’s with EOT of 9Å are shown in Fig. 1 (a) and (b), respectively. Samples which are annealed at high pressure hydrogen and deuterium ambient show increased drive current as well as transconductance. In addition, subthreshold swing was improved after high pressure anneal. In figure 2, the improvement of maximum transconductance value (g_(m,na)) with varying anneal conditions was observed as a function of gate length. The observed g_(m,na) improvement was about 10% and 15% for 10atm and 20atm high pressure anneal respectively.

Reduced threshold voltage shift was also observed in high pressure deuterium annealed sample was shown in figure 6. Threshold voltage shift of FG annealed sample and high pressure hydrogen annealed samples also show similar trend. To evaluate the interface trap density (D_i) for various anneal conditions, fixed-amplitude charge pumping method was used. Interface trap density of forming gas annealed sample was close to 1X10^11cm^-2eV^-1. After high pressure anneal, D_i was around 10^10cm^-2eV^-1. This reduced D_i is analogous to previous work with HfO2 MIS capacitors.[5]

The improvement of transconductance can be attributed to reduced interface trap after high pressure anneal. The degradation of transconductance under constant current stress was shown as a function of stress time in figure 5. The decay slope of FG annealed sample is two times higher than that of high pressure D2 annealed sample. To evaluate the charge trapping characteristics, threshold voltage shift (∆V_G) was monitored under constant current stress. Threshold voltage shift of FG annealed sample and high pressure deuterium annealed sample was shown in figure 6. Reduced threshold voltage shift was also observed in high pressure deuterium annealed sample.

Summary
The effect of high pressure hydrogen and deuterium post-metal anneal on the electrical and reliability characteristics of high-k nMOSFET was investigated. Compared with a forming gas annealed sample, the nMOSFET annealed in high pressure ambient exhibits excellent MOSFET performance and reliability characteristics. It can be attributed to significantly improved interfacial oxide quality and reduction of fast trap sites in high-k layer.

Acknowledgments
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References
Table 1 Process flow of TiN gate nMOSFET

Fig. 1 (a) Drain current (Log I_d and linear I_d) versus gate voltage(V_g), (b) Transconductance (g_m) versus gate voltage(V_g) plot of control and high pressure (H_2 10atm and 20atm, D_2 10atm) annealed sample.

Fig. 2 The improvement of maximum transconductance value (g_m,max) with varying the anneal conditions as a function of gate length.

Fig. 3 Hysteresis effect in the I_d-V_g measurement on the nMOSFET. The range of sweep gate voltage is 0 to 1.5V and 1.5 to 0V, respectively. The threshold voltage shift of FG annealed sample is 11mV and of high pressure deuterium annealed sample is 7mV.

Fig. 4 Interface trap density(D_it) is measured with a fixed-amplitude charge pumping method. V_{amp}=1.2V, freq.=1MHz, rising and falling time =100nsec respectively.

Fig. 5 The degradation of transconductance(g_m,max/g_m,max at fresh) under constant current stress as a function of stress time.

Fig. 6 The threshold voltage shift (ΔV_th) shift under constant current stress as a function of stress time.