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High Quality Hf-Silicate Gate Dielectrics Fabrication by Atomic Layer Deposition (ALD) Technology

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Abstract

We demonstrate high quality HfSiON gate dielectrics fabricated by atomic-layer-deposition (ALD) technology. By using a liquid $SiH[N(CH_3)_2]_3$ precursor, the thickness and composition of ALD Hf-silicate films can be easily controlled with an atomic layer level by the number of Hf/Si deposition ratio. High carrier mobility (same level of universal curves for n- and p-MOSFETs at 0.8MV/cm) and low gate leakage current density (5 ordes of magnitude small than SiO_2) could be obtained using ALD-HfSiON gate dielectrics.

Introduction

High-k dielectric films are required for low power and low leakage current applications. Among many high-k materials, Hf-silicate and its nitride are most promising for high carrier mobility and low leakage current. Therefore, sputter and or MOCVD methods are currently used for Hf-silicate film formation [1-3]. ALD method is desirable for precise control of the composition as well as the film thickness [4]. However, Hf-silicate has not been successfully deposited by ALD method because of the lack of the applicable Si precursor. This paper reports ALD Hf-silicate formation method and the improced electrical characteristics by using the liquid $SiH[N(CH_3)_2]_3$ and $Hf[N(CH_3)(C_2H_5)]_4$ precursors.

ALD Hf-Silicate Formation

Fig.1 shows the thickness of ALD SiO_2 and ALD Hf-silicate films on a Si-substrate as a function of the number of the deposition cycles. In one cycle of the ALD film formation, O_3 was used as a source of oxygen with the concentration of O_3 in O_2 being $100g/Nm^3$. In Fig.1, the number of Hf/Si (=1/1, 1/2, and 1/4) indicates the ratio of HfO_2 and SiO_2 deposition times. In the abscissa, one cycle indicates the sum of HfO_2 and SiO_2 deposition times. For example, one cycle of Hf/Si=1/4 constitutes of one time HfO_2 and 4 times SiO_2 depositions.

As shown in Fig.1, the SiO_2 film thickness increases linearly with ALD cycle with the increment of 0.08nm/cycle. The $SiH[N(CH_3)_2]_3$ precursor makes it possible to deposit the SiO_2 layers not only on SiO_2 films but also on HfO_2 films. Furthermore, the thickness of Hf-silicate films can be easily controlled with an atomic layer level by the number of the deposition cycles. The growth rates of Hf-silicate films are 0.155, 0.222 and 0.373nm/cycle for Hf/Si=1/1 Hf/Si=1/2, and Hf/Si=1/4 ratio, respectively. Fig.2 shows high-resolution RBS spectra of ALD Hf-silicate films, indicating that the Hf/(Hf+Si) compositions are linearly proportional by the number of the Hf/Si ratio. Hf-silicate film compositions can be engineered by changing the number of Hf/Si ratio during ALD cycles. Accordingly, the Hf/(Hf+Si) compositions can be varied from 23 to 56% between Hf/Si=1/1 and 1/4. It is needless to say that a high Hf composition (>60%) is also possible by using high Hf/Si ratio (>1)

Device Fabrication

Fig.3 shows high-k transistor fabrication process flow. The schematic of the high-k gate stack structures are shown in Fig.4. Right after diluted HF treatment, 0.5nm thick SiO_2 layer was formed on 300mm Si wafers using water vapor at 650^{o}C and followed by Hf-silicate film deposition. As shown in Fig. 4(a), 4(b), and 4(c), 1.5nm thick ALD high-k gate films were deposited by using Hf/Si=2/1 (Hf 75%), Hf/Si=4/1 (Hf 85%), and Hf/Si=1/0 (Hf 100%), respectively. In same samples, the high-k gate films were covered by 1.0nm thick ALD-HfSiOx (Hf 56%). As a reference, 2.5nm thick MOCVD Hf-silicate film was also deposited by using HTB and Si_2H_6 precursors [5]. Those high-k gate dielectrics were nitrided using nitrogen radicals [5], and those were annealed in N_2-diluted oxygen atmosphere (O_2 concentration of 0.004%) at high temperatures ranged from 850^{o}C to 1000^{o}C. For the dopant activation, RTA was performed at 1000^{o}C for 3sec.

Electrical Properties

Fig.5 indicates the C-V characteristics of the high-k gate stack MOSFETs (L/W=20/20µm). PDA was performed at 1000^{o}C for 10sec. Flat band voltage (V_{FB}) and the equivalent oxide thickness (EOT) was calculated from C-V curves using EPOQUE [6]. As shown in Fig.5, V_{FB} values were almost same for each high-k gate stack structures for n- and p-MOSFETs. EOT were 1.46nm, 1.47nm, and 1.38nm for ALD HfSiON-1 (Hf 75%), ALD HfSiON-2 (Hf 85%), and ALD HfSiON-3 (Hf 100%) gate structures, respectively. High Hf composition of the high-k gate films (ALD HfSiON-3: Hf 100%) was useful to fabricate the thinner EOT in the same thickness of the high-k gate stack structures. Fig. 6(a) and 6(b) show the effective mobility curves for n-MOS and p-MOSFETs, respectively. As shown in Fig.6, high carrier mobility was obtained for each high-k stack structures for n- and p-MOSFETs, those were same level of universal curve at 0.8MV/cm. These results suggest that the Hf-silicate (Hf 56%) layers of the top of the gate structure are important to obtain the high carrier mobility. Fig.7 shows the dependence of EOT and Vth values on PDA temperature of the ALD HfSiON-3 (Hf 100%) stack structures. By using 850^{o}C PDA treatment, very thin EOT (1.23nm) was fabricated and Vth can be improved for p-MOSFETs.

Fig.8 shows the leakage current density at Vg=1.1V as a function of EOT for n-MOSFET. The leakage current density for MOCVD HfSiON gate stack structures was reduced by more than three orders of magnitude against SiO_2 films. Furthermore, that for ALD HfSiON gate structures was reduced by one order against the MOCVD HfSiON films. Fig. 9(a) and 9(b) show the SIMS depth profiles in the high-k films after PDA treatment of 1000^{o}C for 10sec, for ALD HfSiON/HfO_2 and MOCVD HfSiON stack structures. As shown in Fig.9, the high-k films of carbon and hydrogen concentrations are reduced by ALD method in comparison with MOCVD method. It seems that O_3 treatment is effective to reduce the impurities in one cycle of the ALD film formation, so the leakage current of ALD high-k films is improved.

Summary

High quality HfSiON gate dielectrics formed by ALD Hf-silicate of the liquid $SiH[N(CH_3)_2]_3$ precursor was investigated. The number of Hf/Si deposition ratio makes it possible to control the thickness and composition of ALD Hf-silicate films. High carrier mobility (same level of universal curve for n- and p-MOSFETs at 0.8MV/cm) and the gate leakage current lower than five orders of magnitude against reference SiO_2 films were obtained by the high-temperature PDA just after plasma-nitridation for HfSiON.

References

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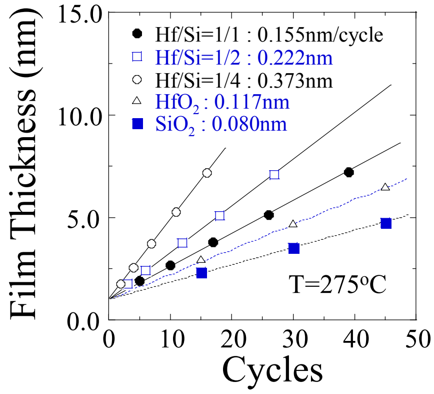

Fig.1 Thickness of ALD-HfSiOx, HfO_2, and SiO_2 films vs. number of deposition cycles.

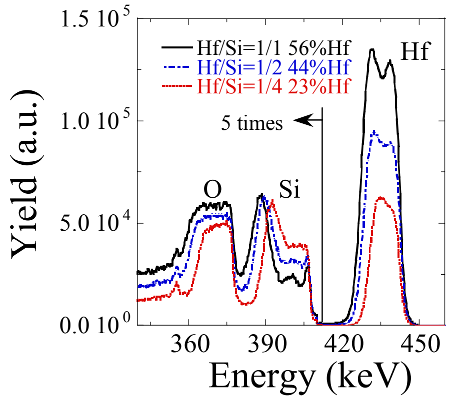

Fig.2 HR-RBS data showing that HfSiOx film compositions can be engineering by ALD cycles.

LOCOS Isolation
Well & S/D formation
S/D pad formation & ILD CVD
Gate trench etching
DHF treatment + SiO_2 (IL) formation
High-k gate stack formation (Fig.4)
Plasma nitridation (N_2 radicals)
PDA treatment
(850-1000°C 0.004%O_2/N_2)
Poly-Si + I/I + Patterning
Activation annealing (1000°C 3sec)
H_2 annealing

Fig.3 Process flow of high-k transistor fabrication.

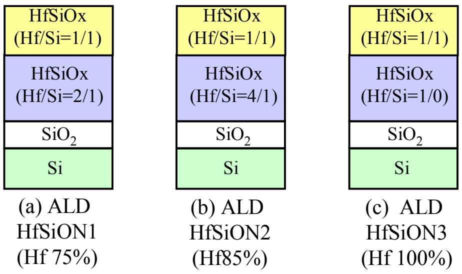

Fig.4 Schematic of the high-k gate stack structures. The high-k gate structures are used to deposit ALD-HfSiOx (Hf/Si=1/1) on the ALD-HfSiOx (Hf/Si=2/1, 4/1, and 1/0).

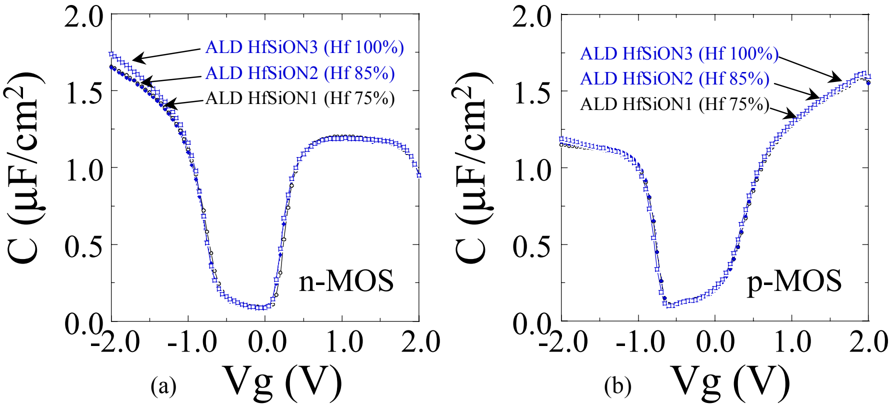

Fig.5 C-V characteristics of the MOSFETs. (a) n-MOS, and (b) p-MOS. PDA was performed at 1000°C for 10sec in 0.004% O_2/N_2 atmosphere.

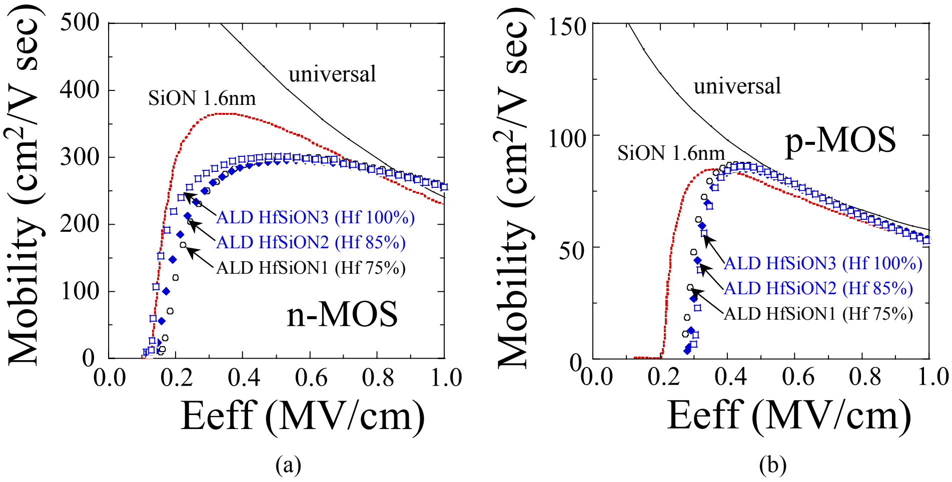

Fig.6 Effective mobilities of the MOSFETs. (a) n-MOSFET, (b) p-MOSFET.

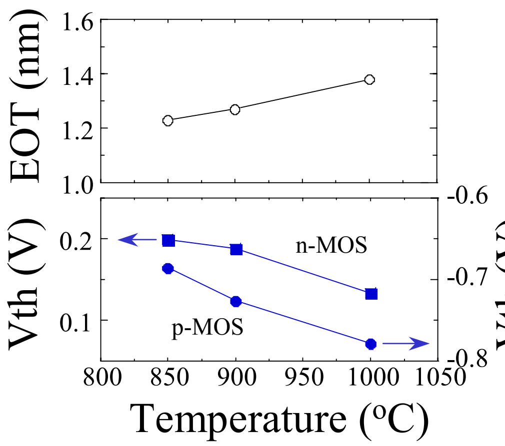

Fig.7 EOT and Vth value vs. PDA temperature of the ALD HfSiON3 (Hf 100%) stack structures.

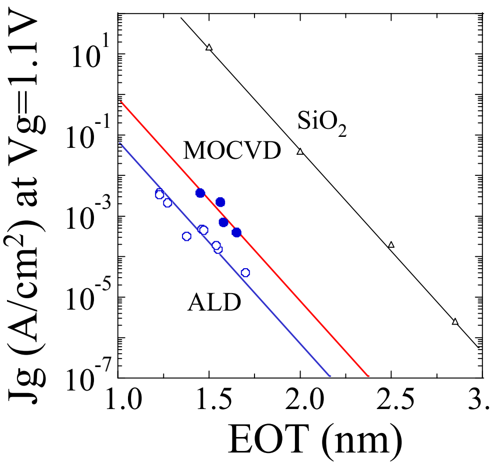

Fig.8 EOT vs Jg at Vg=1.1V (n-MOSFET).

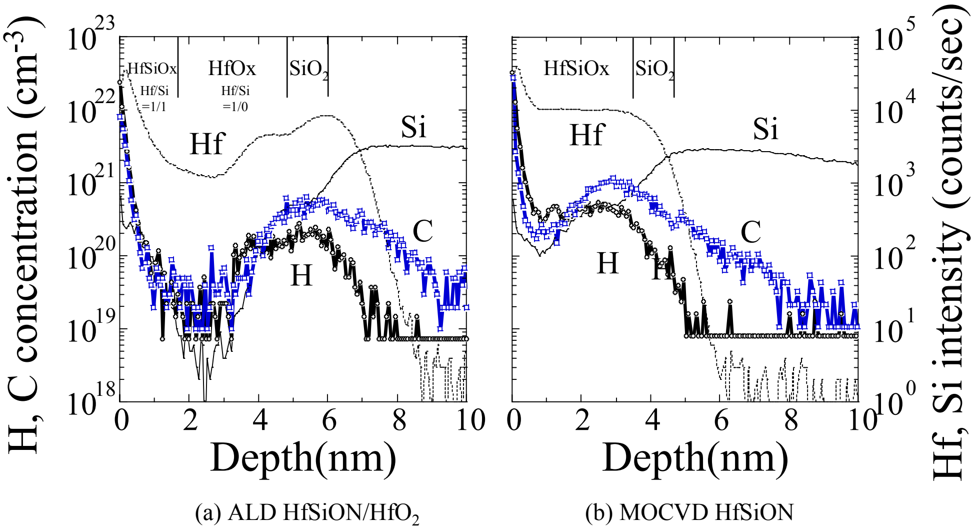

Fig.9 SIMS depth profiles in the high-k films after PDA of 1000°C 10sec.