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A Novel Cell Structure with Bit Line Cap Spacer (BCS) and Top Enlarged Storage Node Contact (TESC) for 90 nm DRAM Technology and Beyond

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1. Introduction

As the design rule is scaled down to sub-100 nm, one of the key technologies in DRAM (Dynamic Random Access Memory) is to obtain the sufficient sensing margin for high performance. It can be improved by increasing a cell capacitance or by decreasing a bit line parasitic capacitance [1]. In our previous works, we have successfully demonstrated a sufficient cell capacitance in 90 nm DRAM technology node with COB (Capacitor Over Bit line) structure using the landing pad to connect storage node contact (SNC) pad with capacitor [2,3]. However, this landing pad layer should need the additional process such as ArF lithography due to the critical landing pad size. In order to solve this issue, the BCS-TESC (Bit line Cap Spacer and Top Enlarged Storage node Contact) process is for the first time proposed and developed. The TESC process can eliminate the landing pad process. The isotropic characteristic of wet etching strongly determines the SNC pad size and the mechanical stability of capacitor. And the BCS process, another key feature of this novel scheme, can decrease the bit line parasitic capacitance by forming the oxide sidewall spacer along the bit line, resulting in contributing for a high performance.

In this paper, the key technologies of the BCS-TESC scheme are described in detail with 90 nm technology node. And the BCS-TESC scheme has demonstrated with 512Mb DDR DRAM.

2. Process Integration

Bit line Cap Spacer formation technology

The process flow for the BCS and the TESC is described in Table I. The schematic diagram of an overall BCS-TESC process is shown in Fig. 1. After bit line (BL) pattern is formed, the HDP (high density plasma) oxide as a part of ILD (interlayer dielectric) layer is deposited and partially etched back until exposing the bottom level of BL mask as shown in Fig. 2. Then, 400 Å silicon nitride is deposited on exposed BL mask and subsequently etched back using dry etching. Because the SAC (self-aligned contact) process is adopted to form SNC, it is needed to have sufficient thickness of BCS during SNC formation. After then, additional HDP oxide deposition is sequentially followed by CMP (chemical mechanical polishing), capping HDP oxide and poly-silicon deposition as a mask layer, as shown in Fig. 3. The gap-fill capability of the BCS scheme is increased due to the lower aspect ratio with respect to the conventional scheme.

Top Enlarged Storage Node Contact formation Technology

After the SNC patterning is performed using KrF lithography, mask poly-silicon is firstly etched away and a part of ILD layer is also removed by dry etching until exposing the BL mask. After then, the top enlarged process using wet etching, the most key technologies in this work, is performed, which determines a SNC pad size to connect with a capacitor. Fig. 4 and Fig. 5 show the cross-sectional SEM images just after enlargement along the direction of word line and bit line, respectively. An enlarged amount should be controlled strictly in order to obtain the sufficient pad area and prevent the bridge between SNC pads along BL direction. We should also note that the sidewall oxide underneath the BCS is not consumed during the enlargement process in order to decrease the BL parasitic capacitance (Cbl). Fig. 6 shows the cross-sectional SEM image after SNC formation. It is clearly seen that a sufficient sidewall profile is obtained. The remained oxide is critically controlled because the thickness of sidewall depends on the mask nitride loss that occurs during the SNC etching. In novel scheme, the ILD oxide etching process consists of two steps. First, using wet etching the oxide is partially etched with high selectivity to nitride spacer. The remaining oxide is subsequently etched until exposing the SNC bottom level using dry etching. As a result, the sufficient sidewall spacer is obtained. Fig. 7 shows the cross-sectional SEM image of TESC, where the sufficient pad area is achieved in order to fully overlap between pad and capacitor. Therefore, it is possible to remove the additional landing pad lithography. Fig. 8 shows the top-view SEM image of separated SNC pad using etch-back and CMP process. Fig. 9 shows the cross-sectional SEM images of fully integrated 512Mb DRAM cell array with 90 nm technology. Fig. 10 shows the schematic diagram of (a) conventional SNC scheme and (b) BCS-TESC scheme, respectively. To maximize cell area, it is inevitable to use the landing pad in the conventional scheme. However, the BCS-TESC scheme can easily obtain the full overlap to SNC without landing pad as shown in Fig. 10(b). Furthermore, it can decrease the Cbl using oxide spacer.

Device Characteristics

Fig. 11 shows the distribution of the BL parasitic capacitance with respect to SNC structure. The BL parasitic capacitance of BCS-TESC scheme is decreased by about 10 %. This is because the sidewall material of BCS-TESC structure is SiO_2 (k = 3.9) instead of Si_3N_4 (k = 7). Fig. 12 shows the distribution of the breakdown voltage between storage node and bit line with respect to SNC structure. The breakdown voltage is slightly increased compared to that of the conventional scheme. In our simulated data by H-SPICE simulator code, the charge sharing time (tCS) is increased by 0.3 ns with respect to BL loading capacitance as shown in Fig. 13. Fig. 14 shows the Shmoo map of the RAS to CAS delay time (tRCD) with respect to (a) BCS-TESC scheme and (b) conventional SNC. It is clearly seen that the tRCD is improved by 0.5 ns using BCS-TESC.

3. Conclusions

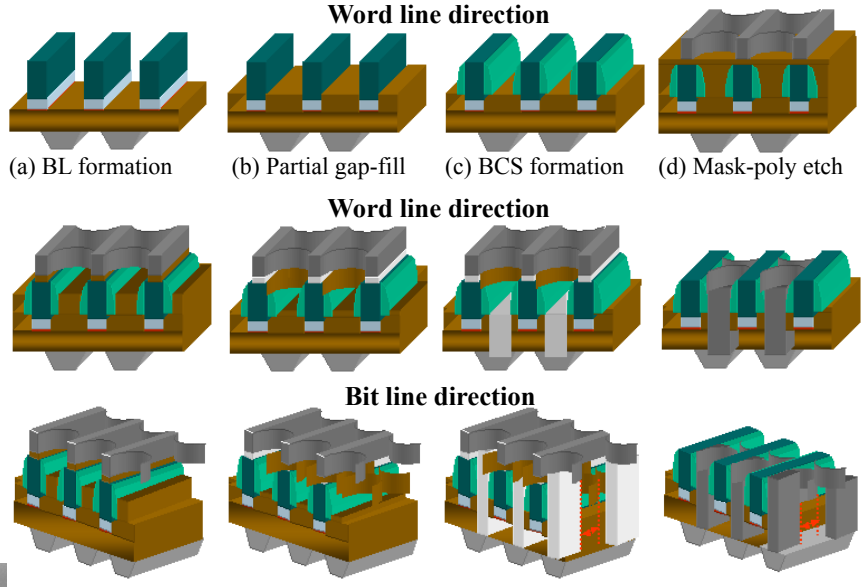
For the first time, the BCS-TESC process is successfully developed using 90 nm DRAM technology. With this novel scheme, we eliminate a critical ArF lithography for the landing pad to connect the SNC pad with the capacitor, resulting in the cost-effective process. Furthermore, we decrease the BL parasitic capacitance by about 10 %. The BCS-TESC scheme will be one of the most promising technologies in sub-100 nm technology era.

References

[1] B.J. Park et al., Symp. on VLSI Tech., p.182-183, 2002.
[2] Y.K. Park et al., IEDM Technical Digest, p.819-822, 2002.
[3] Jaegoo Lee et al., Symp. on VLSI Tech., p.57-58, 2003.

Table I. Process flow of BCS-TESC

Process	Process features
Bit Line Cap Spacer ***(BCS)***	▪W Bit line patterning with ArF lithog. ▪Partial ILD fill with HDP ▪Cap Spacer SiN dep. and etch back ▪Fully fill ILD with HDP ▪Mask-poly dep. before the SNC lithog.
Top Enlarged SNC ***(TESC)***	▪SNC patterning using KrF lithog. ▪Mask poly etching ▪ILD partial etching around 700 Å ▪ILD wet etching ▪ILD etching until the SNC pad ▪Poly deposition ▪Poly etch back and CMP



(a) BL formation (b) Partial gap-fill (c) BCS formation (d) Mask-poly etch

(e) Partial ILD etch (f) Top enlargement (g) 2nd ILD etch (h) SNC pad separation

Fig. 1 Schematic diagram of the BCS-TESC process.

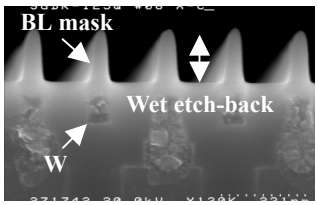


Fig. 2 Cross-sectional view of partial ILD gap-fill.

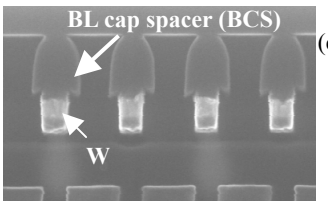


Fig. 3 Cross-sectional view of BL cap spacer (BCS).

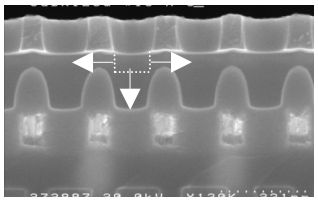


Fig. 4 Cross-sectional view of wet enlargement along word line direction.

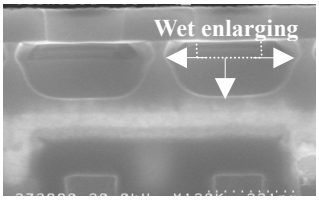


Fig. 5 Cross-sectional view of top enlarged SNC along bit line direction.

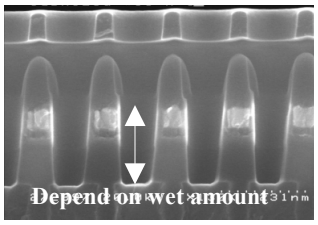


Fig. 6 Cross-sectional view of the BCS-TESC in the direction of word line.

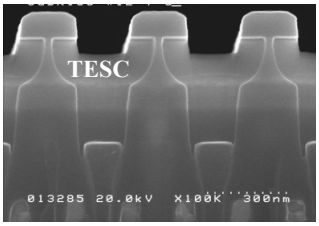


Fig. 7 Cross-sectional view of the BCS-TESC in the direction of bit line.

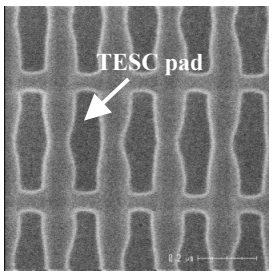


Fig. 8 Top view image of the complete BCS-TESC pads after node separation.

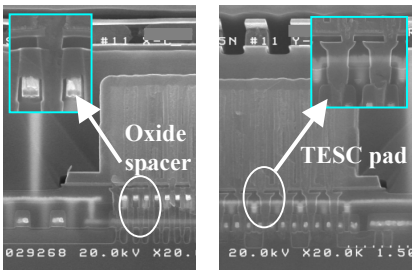
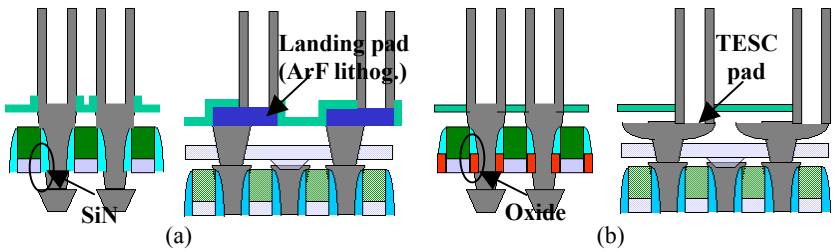


Fig. 9 Cross-sectional view of fully integrated DRAM using the BCS-TESC scheme.



(a) (b)

Fig. 10 Schematic diagram of (a) the conventional scheme and (b) the BCS-TESC scheme.

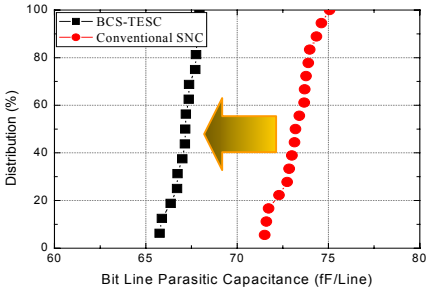


Fig. 11 Distribution of the bit line parasitic capacitance. BCS-TESC shows the superior characteristic.

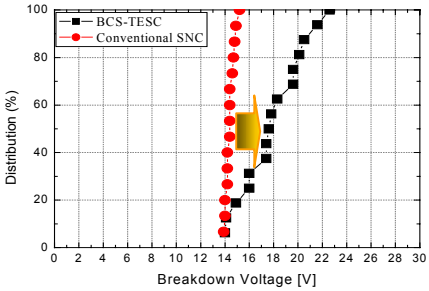


Fig. 12 Distribution of the break-down voltage between storage node and bit line.

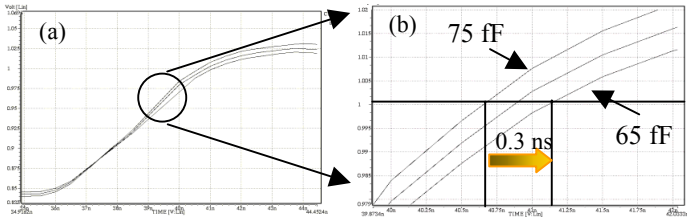
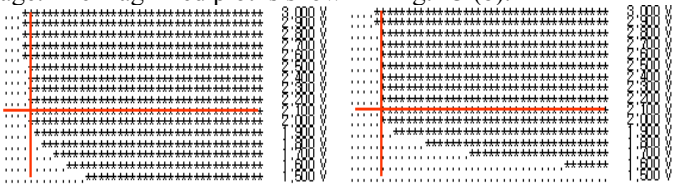


Fig. 13 Simulated tCS with respect to charging sharing voltage. The magnified plot is shown in Fig. 13 (b).



(a) BCS-TESC scheme (b) Conventional scheme

Fig. 14 Shmoo map of the tRCD with respect to (a) BCS-TESC and (b) conventional SNC.