Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 212-213

C-3-1

Experimental Clarification of Hydrogen-related Mechanism in NBT Degradation

Yuichiro Mitani and Hideki Satake*

Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone : +81-45-770-3689 Fax : +81-45-770-3578 E-mail : mitani@amc.toshiba.co.jp

1. Introduction

Negative bias temperature instability (NBTI) has become increasingly serious in the context of efforts to realize highly reliable integrated CMOS devices, because of the severe degradation of threshold voltage shift and interface-state generation [1]. The threshold voltage shift is generally attributed to the creation of interface traps and positive fixed charges consequent on the dissociation of Si-H bonds at Si/SiO_2 interface by holes, and subsequent diffusion of the released hydrogen-related species towards the gate electrode [2-7]. According to this reaction- diffusion (R-D) model [6, 7], threshold voltage shifts are dominated only by the quantity of the released hydrogen atoms from Si/SiO_2 interface. However, the experimental evidence concerning the validity of this R-D model has not been sufficiently obtained yet.

In this work, in order to clarify the correlation between NBTI and hydrogen which is released from SiON/Si interface, the effect of H_2 ambient annealing on NBT degradation and the recovery was investigated.

2. Recovery of NBTI by H_2 Annealing

Fig. 1 shows the recoveries of the threshold voltage shift (ΔV_{TH}) and the increment of charge-pumping current (ΔI_{CP}) for several annealing condition after NBT stress during 640 sec. Recoveries of ΔV_{TH} and ΔI_{CP} are observed under the condition without any annealing (***A*** in Fig. 1). The recoveries are enhanced with using N_2 ambient annealing (***B*** in Fig. 1). Surprisingly the degradations are completely recovered with the H_2 ambient annealing (***C*** in Fig. 1).

The recovery with H_2 ambient annealing is available for the periodical NBT stress as shown. Figure 3 shows the reciprocal characteristics of degradation and recovery of ΔV_{TH} and ΔI_{CP}. Namely, the NBT measurement and H_2 annealing were repeated alternately as shown in Fig. 2. Note that ΔV_{TH} and ΔI_{CP} values of H_2-annealed devices completely coincide with those in the case of the first NBT stress, irrespective the number of both the stress time and the H_2 annealing time. That is, NBTI leaves no trace in gate oxides and these interfaces after H_2 annealing. This result indicates that the defects generated by applying NBT stress can be completely recovered by hydrogen incorporation.

3. Correlation between ΔV_{TH} and ΔI_{CP}

Next, we have verified whether the NBT degradation is dominated only by the hydrogen release from the Si/SiO_2 interface. It was reported that the forming gas annealing condition has an effect on NBTI [8]. Therefore, in order to verify the NBT degradation model concerning hydrogen, the devices which were annealed respectively in the different condition have been utilized.

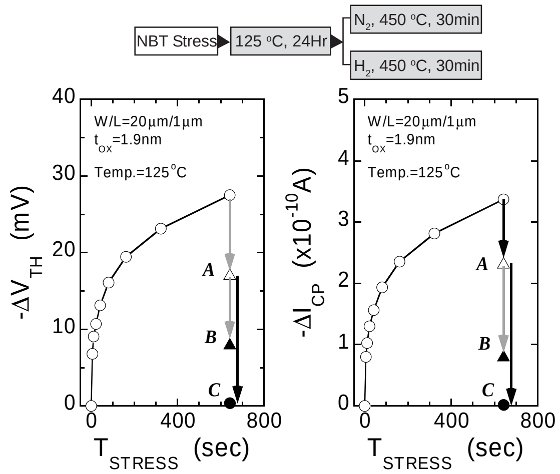

Fig. 1 Typical ΔV_{TH} and ΔI_{CP} degradation as a function of stress time. ΔV_{TH} and ΔI_{CP} were recovered (***A***) at 125 °C for 24 hours in the measurement system, (***B***) by annealing in N_2 ambient at 450 °C, and (***C***) by annealing in diluted H_2 ambient at 450 °C. Note that NBTI is completely recovered by H_2 annealing.

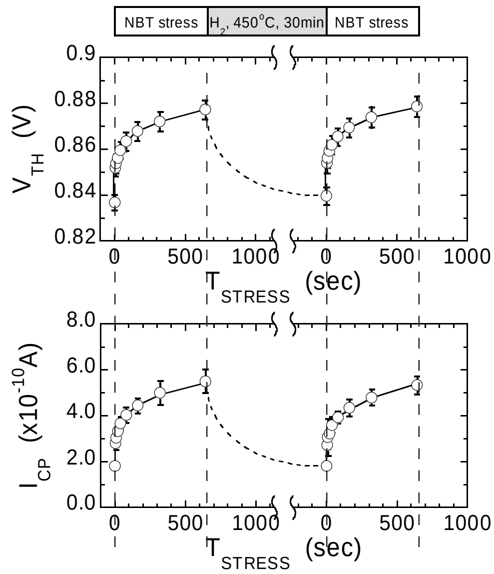

Fig. 2 V_{TH} and I_{CP} before and after H_2 annealing. H_2 annealing was performed at 450 °C for 30 min. The degradation behavior under 2nd NBT stress was completely the same as that under 1st NBT stress.

Fig. 4 shows the average ΔI_{CP} after NBT stress as a function of the initial (prestressed) I_{CP} values. It should be noted that ΔI_{CP} is independent of the initial I_{CP}, i.e. the annealing condition. On the other hand, ΔV_{TH} does not coincide among three kinds of the devices in spite of the same ΔI_{CP}, as shown in Fig.

*Present address: MIRAI Project, Association of Super-Advanced Electronics Technologies (ASET),AIST
Tsukuba West 7, Tsukuba, 305-8569, Japan

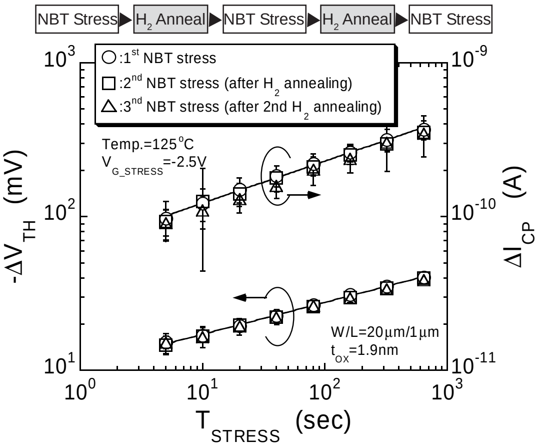

Fig. 3 ΔV_{TH} and ΔI_{CP} as a function of the stress time. ΔV_{TH} and ΔI_{CP} of H_2-annealed devices completely coincide with those in the case of 1st NBT stress.

5. It was found that ΔV_{TH} values of the devices which were annealed at 450 °C is larger than that in the case of hydrogen annealing at 400 °C. In addition, Fig. 6 shows the correlation between ΔI_{CP} and ΔV_{TH} of these devices. It has been reported that ΔV_{TH} strongly depends on the interface-state generation under NBT stress [9, 10]. From the result in Fig. 6, it was found that higher temperature annealing enhances the V_{TH} degradation, even if the same quantity of the interface-states was generated as shown in Fig. 4. These experimental results as shown in Figs. 4-5 indicate that ΔV_{TH} under NBT stress depends on not only the quantity of released hydrogen from Si/SiO_2 interface, i.e. the R-D model. The additional mechanism for the ΔV_{TH} enhancement has not been clarified yet. However, from the experimental results in this work, it can be concluded at least that the traps (or the defects) which enhance ΔV_{TH} are unrelated to the released hydrogen from Si/SiO_2 interface, but these can be completely vanished by hydrogen incorporation. Furthermore, it is inferred that this additional NBT degradation depends on the temperature of the forming gas annealing.

4. Conclusion

In this work, the correlation between hydrogen and NBT degradation have been investigated. As a result, it was found that ΔV_{TH} and ΔI_{CP} after NBT stress are completely recovered by H_2 annealing and no trace is left. On the other hand, ΔV_{TH} depends on the annealing condition, in spite of the same quantity of generated interface-states. From these experiments, it can be concluded that the defects generated by applying NBT stress is completely repaired by hydrogen incorporation, but the additional mechanism of V_{TH} shift which is unrelated to the released hydrogen from the gate oxide interface is also involved with NBTI.

Acknowledgments

The authors would like to thank Dr. Kazuya Matsuzawa for his useful suggestion and discussion.

References

[1] N. Kimizuka *et al.* :VLSI Symp. Digest, 73, 1999.
[2] N. Kimizuka *et al.* :VLSI Symp. Digest, 92, 2000.
[3] G. La. Rosa *et al.*: IRPS proc., 73, 1999.
[4] T. Yamamoto *et al.* : IEEE ED-46, 921, 1999.

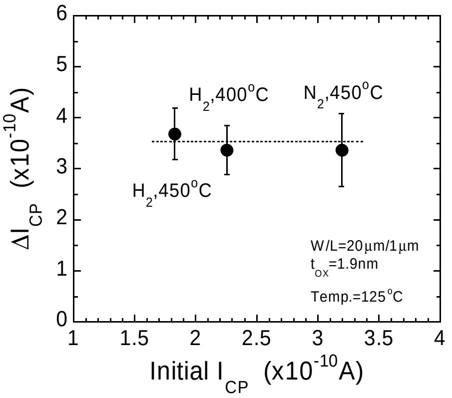

Fig. 4 Increment of charge-pumping current (ΔI_{CP}) under NBT stress. Devices were applied NBT stress for 680 sec at V_G=-2.5 V. Note that ΔI_{CP} is not affected by annealing, condition, irrespective of the initial I_{CP}.

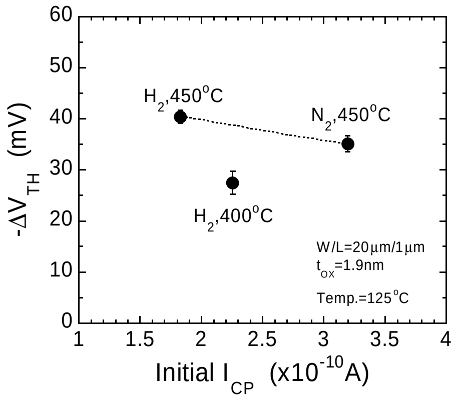

Fig. 5 Threshold voltage shift (ΔV_{TH}) under NBT stress. Devices were applied NBT stress for 680 sec at V_G=-2.5 V. It was found that ΔV_{TH} value depends on both hydrogen-annealing temperature and initial I_{CP}.

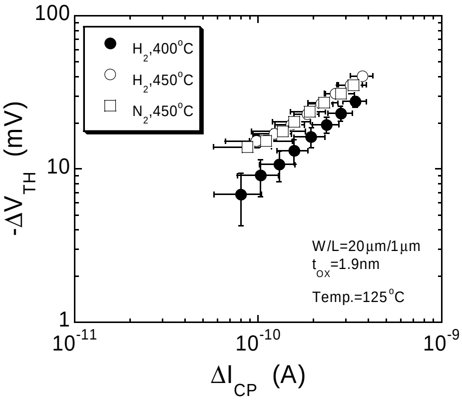

Fig. 6 Correlation between ΔI_{CP} and ΔV_{TH}. Note that, in the case of ΔI_{CP}-ΔV_{TH} correlations of the devices which are annealed at 450 °C are clearly split from the case of the device annealed at 400 °C.

[5] G. J. Gerardi *et al.* : J. Electrochem., 2609, 1989.
[6] M. A. Alam : IEDM, Tech. Digest, 345, 2003.
[7] S. Mahapatra et al. : IEDM, Tech., Digest, 337, 2003.
[8] E. Morifuji *et al.* : VLSI Symp. Digest, 218, 2002.
[9] Y. Mitani *et al.* : IEDM, Tech. Digest, 509, 2002.
[10] S. Mahapatra *et al.* : IEDM, Tech. Digest, 337, 2003.