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Ultra-Short Pulse I-V Characterization of the Intrinsic Behavior of High-κ Devices

Chadwin D. Young[1], Yuegang Zhao[2], Michael Pendley[1], Byoung Hun Lee[1,3], Kenneth Matthews[1], Jang Hoan Sim[1], Rino Choi[1], Gennadi Bersuker[1], and George A. Brown[1]

Tel: 512-356-3612, Fax: 512-356-7640, e-mail: chadwin.young@SEMATECH.org
[1]International SEMATECH, [3]IBM and Assignee, 2706 Montopolis Dr, Austin, TX, 78741, U.S.A.
[2]Keithley Instruments, 30500 Bainbridge Road, Cleveland, Ohio, 44139, U.S.A.

1. Introduction

V_t instability, mobility degradation, and reliability are key issues in the evaluation of implementing high-κ gate dielectrics. Recent studies on transient charge trapping indicate that these issues are actually closely related to each other. Transient charge trapping of high-κ gate dielectrics and their relaxation are found to be major sources of device instability, and the impact of these phenomena on reliability evaluation has been studied [1-5]. The trap centers can be "charged" and "discharged" relatively fast, and they adversely affect the results of conventional DC approaches (i.e., $I_d - V_g$ and $I_d - V_d$), which impact mobility [6].

To evaluate the intrinsic nature of the high-κ gate stack, new measurement methodologies that attempt to measure the intrinsic characteristics of high-κ gate dielectric structures in the absence of trapped charge are necessary.

In this work, an ultra-short pulse measurement will be utilized to demonstrate the impact of transient charging on DC I_d-V_g measurements, and it will be shown that a significant portion of mobility degradation observed in high-κ devices is actually due to measurement error originating from transient charge trapping during the DC measurements.

2. Methodology

Fast transient (i.e., short pulse) measurement and analysis has been studied to address the need for improved characterization strategies [7, 8]. However, transient charge trapping has been found to affect DC measurements that can occur within the order of μsec [1]. Thus, to investigate the intrinsic properties of high-κ gate stacks with minimal charge trapping, a significantly faster measurement than previously reported is needed. The concept of the high speed pulsed I-V measurement was first introduced and used to study the self-heating effect in SOI MOSFETs [9] where K. Jenkins, et al., demonstrated: 1) the use of a 10nsec pulse to make self-heating negligible, and 2) the pulsed performance of SOI devices is superior to DC characteristics. This method can be adapted to characterize the I_d–V_d, I_d–V_g characteristics of high-κ devices with very short pulse durations to minimize or eliminate the effect of fast charge trapping. Fig. 1 shows a diagram of the system configuration where a Keithley Model 4200-SCS provides the DC bias as well as the control of the pulse generator and the digital scope via GPIB. In the pulse I-V ramp measurement, a train of continuous pulses, with duty cycle well below 0.1%, is produced. The drain current is extracted from the amplitude of the response pulse voltage at the drain terminal. Fig. 1 illustrates a screen shot of the input and output pulses from the scope where the output can be converted to I_d and plotted versus V_g to create the single

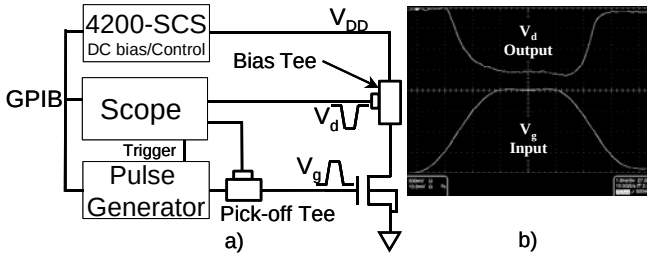

Fig. 1. a) Experimental setup using a MOSFET in an inverter configuration. b) "Screen shot" of the input (V_g) and output (V_d) waveforms for the configuration ($t_r = t_f$=2ns, pulse width = ~5 ns)

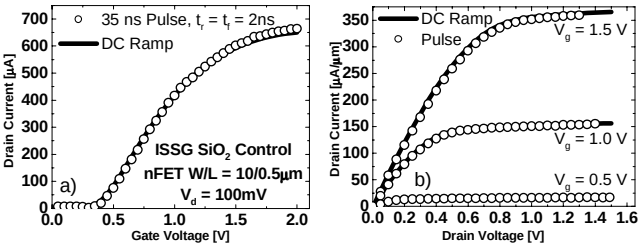

Fig. 2: Benchmark comparison of "ramped" pulse I-V and DC I-V in conventional: a) I_d-V_g and b) I_d-V_d characteristics for 2 nm SiO_2.

pulse measurement result in Fig. 3. Multiple pulses can be averaged for optimized resolution. Pulse amplitude degradation along the path of ultra short pulse was calibrated using a MOSFET with a SiO_2 gate dielectric that shows no charge trapping behavior as shown in Fig. 2. Fig. 2 demonstrates an example calibration on a 2 nm *in-situ* steam generated (ISSG) oxide.

For this study, an ~1 nm chemical oxide interfacial layer (IL) with a 3 nm Atomic Layer Deposited (ALD) HfO_2 gate dielectric upon the IL was fabricated using conventional planar CMOS processing with a source/drain activation done at 1000°C for 10 sec.

3. Results and Discussion

Transistors with W/L = 10/0.5 μm were subjected to short pulse measurements as outlined in section 3 and [7, 8]. "Single pulse" (SP) I_d-V_g measurements were done with t_r= t_f= pulse width (PW). Each SP measurement started and ended at $V_g \pm 1$ V as the discharge condition for nMOS and pMOS, respectively, with the top of the pulse taken to achieve a $|V_g$-$V_t|$ match in inversion. A difference between the I_d-V_g curves generated by the up and down swing of V_g reflects the effect of the charge trapping (Fig. 3). As illustrated in Fig. 3, charge trapping increased as gate bias increased further into inversion for the nMOS case while pMOS trapping is negligible. The pulsed data superimposed with the nMOS DC $I_d - V_g$ characteristic demonstrates

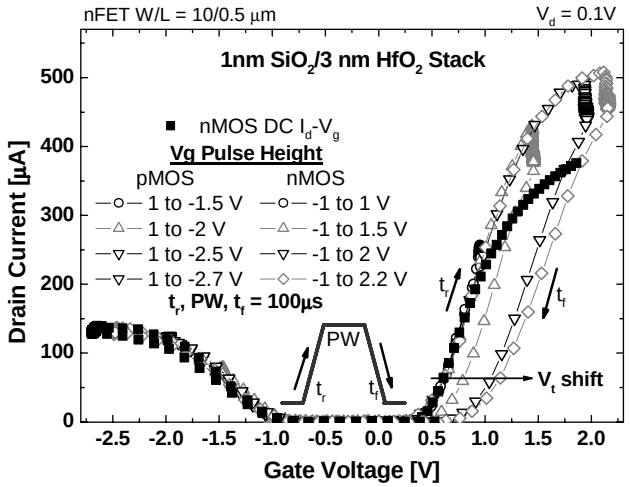

Fig.3. "Single Pulse" I_d-V_g characteristics for different inversion biases illustrating increased trapping (V_t shift) with increased inversion bias for nMOS and negligible trapping for pMOS. The included nMOS DC ramp I_d-V_g result demonstrates the effect of charge trapping during the slower measurement.

that the latter degraded due to charge trapping during the slow V_g ramp up in the DC measurements.

This SP result can also be evaluated versus time to demonstrate the effect of an inversion bias condition that is applied to a nMOSFET. Fig. 4 (b) illustrates the effect of increased charging with longer pulse widths which result in degraded drive currents due to the channel electron loss and V_{th} shift [7]. On the other hand, drain current trace from ultra short pulse shows a negligible current degradation, indicating the transient charging effect is not significant in this time scale (Fig. 4 (a)). Thus, using this ultra-short pulse, "close-to-intrinsic" characteristics of high-κ gate stacks can be investigated. In this work, HfO_2 NMOS showing serious mobility degradation is chosen to show the difference between DC measurement and pulse I-V measurement. Fig. 5 clearly illustrates the effect of using a ramped pulse a) $I_d - V_g$ and b) $I_d - V_d$ compared to its conventional DC counterpart and Fig. 5b illustrates the load line effect [9] where the pulsed I_d current does not extend to match the DC V_d sweep. The difference between DC measurement and pulsed I-V measurement suggests that the intrinsic mobility and transconductance of HfO_2 NMOS is much higher than what has been measured with DC measurement.

4. Conclusions

Close-to-intrinsic characteristics of high-κ devices are obtained using a high speed pulsed I-V methodology. With a 35 nsec pulse width, the saturation current of this high-κ sample has increased by as much as ~40% at high V_g. This result indicates that transient charging during DC I_d-V_g measurement considerably influences a significant portion of the crucial DC mobility degradation observed thus far. According to this understanding, high-κ gate dielectrics could be implemented in the portion of the circuit where charge trapping can be minimized, for example, high frequency and low duty cycle circuits. Also, this method can be utilized to investigate the intrinsic reliability

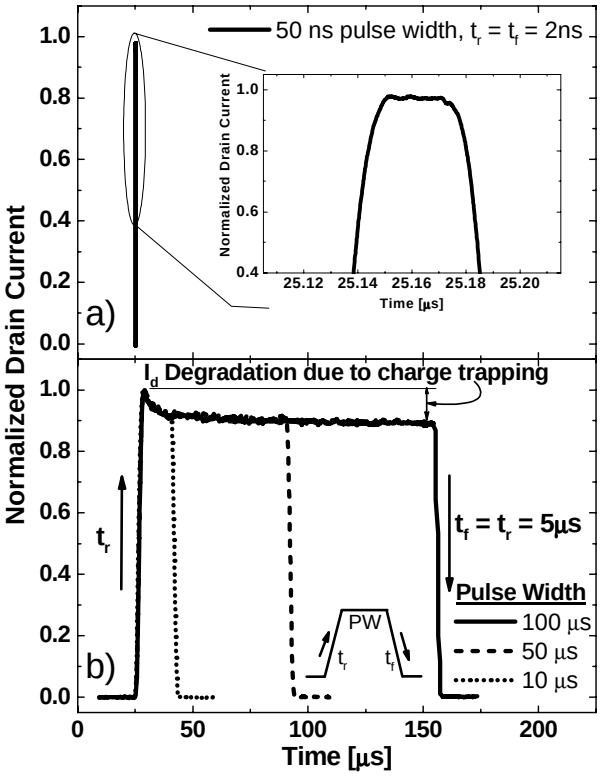

Fig. 4: Pulsed I_d versus time characteristics illustrating the degradation in drive current over time due to channel electron trapping in the high-k. a) Pulse width = 50 ns, void of trapping; b) pulse width = 100 μs, 50 μs, and 10 μs, subject to charge trapping.

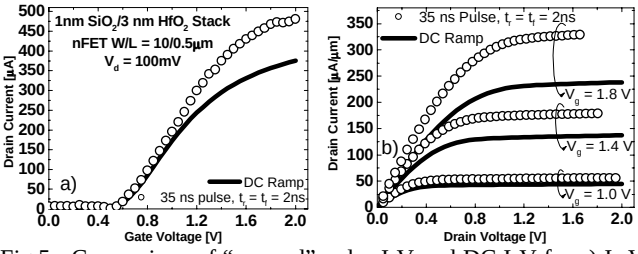

Fig.5: Comparison of "ramped" pulse I-V and DC I-V for a) I_d-V_g and b) I_d-V_d characteristics on high-κ gate illustrating the improved drive current results for the pulsed methodologies.

characteristics of high-κ devices, which is as important as mobility issues.

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References

[1] B.H.Lee et al., *Submitted to SSDM*, 2004
[2] R.Choi et al., *to be presented at DRC*, 2004
[3] J.H.Sim et al., *to be presented at DRC*, 2004
[4] E.Gusev *et al., Appl. Phys. Lett.*, (2003), p. 5223
[5] B.H. Lee *et al., IRPS* (2004), p. 691
[6] C.D. Young, et al., *Fall ECS*, **PV 2003-22**, p. 347, Oct. 2003
[7] C.D. Young, et al., *IRPS*, p. 597, March 2004
[8] A. Kerber, et al., *IRPS*, p. 41, March 2003
[9] K. A. Jenkins, et al., *IEEE TED*, vol. 44, No. 11, p. 1923, 1997