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Advantages of Ge (111) Surface for High Quality HfO_2/Ge Interface

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1. Introduction

Germanium CMOS is historically one left behind, but recently its research has come to life again from the trend of using deposited high-k film than thermally grown SiO_2 for further scaling [1), 2)]. Furthermore, it is quite important to investigate which surface orientation of Ge is more appropriate for MISFET performance, as deeply investigated in silicon. From the performance point of view, the surface orientation is a hot issue in terms of Ge band structure [3)]. On the other hand, we found that chemically and thermodynamically unstable characteristics of Ge surface significantly affect the interface layer formation and the surface reaction during high-k deposition and thermal treatments [4)].

The purpose of this study is to clarify surface orientation effects on high-k/Ge MIS system through physical and electrical characterizations. In particular, this paper focuses on HfO_2 on Ge (100) and (111) wafers.

2. Experimental

p-type Ge (100) and (111) wafers were simultaneously processed for MIS capacitors. Wafer cleaning steps are listed in **Table 1**. Although this process has not been optimized, it is noted that all of the processes were conducted simultaneously in a same manner for both wafers.

Table 1 Cleaning process of Ge wafers before HfO_2 deposition.

Ge cleaning	1. Degreasing by methanol. 2. Native oxide removal by HCl:DI (1:4). 3. Re-oxidization in H_2O_2:NH_3 :DI (2:1:20). 4. Dipping in diluted HF solution (5%) 5. DI water rinse

The HfO_2 films were deposited by two-step sputtering of Hf target. First metallic Hf was deposited in Ar flow, followed by HfO_2 deposition in Ar/O_2 flow. The predeposited metallic Hf layer is oxidized during the reactive sputtering process, and expected to restrict the interface layer formation. The films were annealed in N_2 and O_2 ambient, at the temperature ranged from 400ºC to 650ºC. Finally, Au electrodes were deposited on the HfO_2 films on both Ge samples.

For the physical analysis, atomic force microscope (AFM) for surface roughness, spectroscopic ellipsometry for Ge oxide thickness, and glazing incidence x-ray reflectivity (GIXR) for HfO_2 thickness were used, while C-V measurements were used for electrical analysis.

3. Results and Discussion

3.1. Ge (100) and (111) surfaces after O_2 treatment

First, oxidation rate of Ge surface was investigated. **Fig. 1** shows the oxidation rate difference on Ge (100) and (111) wafers. The results on Si (100) and (111) wafers are also shown in the figure. Here, it should be noted that Ge oxidation sharply starts around 450 ºC, and that Ge (111) shows a lower oxidation rate than Ge (100). This fact means that Ge (111) wafer is tougher than Ge (100) against the O_2 attack. Next, HfO_2/Ge samples were annealed in O_2, followed by removing the surface HfO_2 film. Then, the top surfaces of Ge wafers were investigated by AFM. **Fig. 2 (a)** and **(b)** show AFM images and RMS of surface roughness after removing HfO_2, respectively. It is clearly seen that Ge (100) is more roughed than Ge (111). This result is quite important in terms of the selection of Ge wafer orientation for device fabrication.

3.2 Electrical measurement of HfO_2/Ge MIS capacitors

Figure 3 shows a difference of interface quality of Au/HfO_2/Ge MIS capacitors between on Ge (100) and on Ge (111). By annealing at 400ºC, no difference is observed in C-V characteristics, while by annealing at 650ºC a significant stretched-out is observed for the C-V

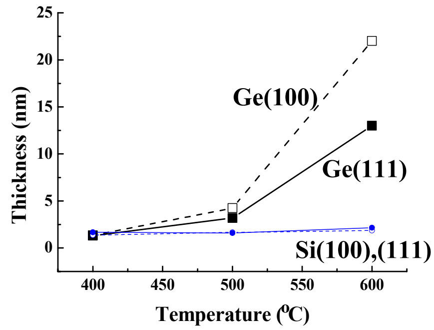

Fig. 1 Comparison of oxidation rates between Ge(100) and Ge (111) surfaces. The results for Si (100) and Si (111) surfaces are also shown (no substantial oxidation).

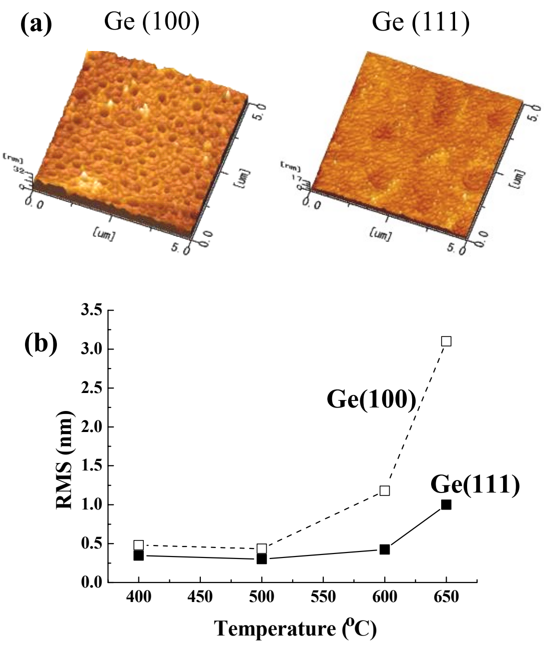

Fig. 2 The interface roughness comparison of HfO_2/Ge(100) with HfO_2/Ge(111). The Ge surfaces were observed by AFM after removing HfO_2 films. **(a)** AFM images of the 650ºC annealed samples for 5×5μm^2 area in the same scale. **(b)** RMS of the surface roughness.

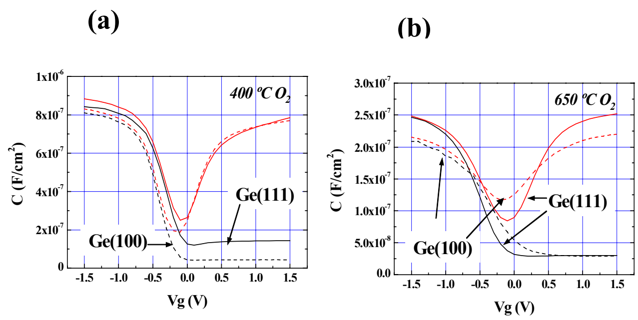

Fig. 3 C-V characteristics in Au/HfO_2/Ge(100) (broken lines) and HfO_2/Ge(111) (solid lines) MIS capacitors measured at 1kHz and 1MHz. **(a)** annealed at 400 ºC in O_2 for 30sec, and **(b)** annealed at 650 ºC in O_2 for 30 sec.

characteristics of HfO_2/Ge (100) both in 1kHz and 1MHz measurements. This fact implies that the interface on Ge (100) is intrinsically degraded from electrical as well as morphological viewpoints. The annealing temperature and ambient effects on Ge (100) wafers are shown in **Fig. 4**. The stretched-out effect seems worse at higher temperature or in N_2 ambient. Thus it is concluded that the annealing at higher temperature and in N_2 ambient significantly degrade the HfO_2/Ge(100) interface.

Finally, we discuss a difference of CET of HfO_2 MIS capacitors between on Ge (100) and that on Ge (111), with PDA in O_2. **Fig. 5** shows the CET as a function of PDA temperature for HfO_2/Ge(100) and HfO_2/Ge(111).

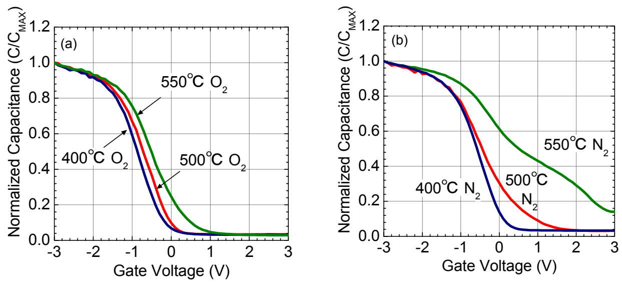

Fig. 4 1MHz C-V characteristics of Au/HfO_2(8nm)/p-Ge MIS capacitors, annealed at 400ºC, 500ºC, and 550ºC in **(a)** O_2 and **(b)** N_2 ambient. The vertical axis is normalized by the maximum capacitance value. The interface degradation occurs significantly by N_2 annealing at high temperature.

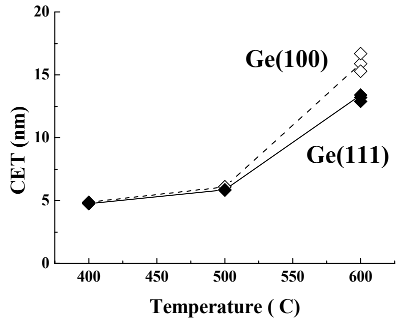

Fig. 5 CET difference between HfO_2 MIS capacitors simultaneously processed on Ge (100) and (111) wafers. A significant CET difference at 600ºC is probably due to the oxidation rate difference between Ge(100) and Ge(111) surfaces as shown in Fig.1.

Since the oxidation rate on Ge (100) is higher than that on Ge (111) as shown in Fig.1**,** the resultant CET on Ge (111) is thinner than that on Ge (100). We have reported that HfO_2 on Ge has thinner CET than that on Si in a certain HfO_2 deposition condition [4)]. The present results show a further advantage of using Ge (111) wafer.

4. Conclusions

Several advantages of Ge (111) for HfO_2/Ge interface have been demonstrated. In addition to the advantage of low field mobility in MISFET, it is strongly suggested that Ge (111) has a promising properties from the viewpoint of device and process stability in the combination of high-k dielectrics.

Acknowledgements

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