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SOI Floating Body Memories for Embedded Memory Applications

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1. Introduction

Recently new concepts have been proposed to address the scaling and performance limitations found in standard embedded RAM memories. A capacitor less RAM cell on SOI is simpler, uses only conventional materials and is therefore fully compatible with CMOS processes. A first complex version integrating two transistors has been described in [1]. By exploiting the Floating Body (FB) effect of a single MOSFET, a simpler and denser structure was proposed by Tack et al. [2]. The device operation was however not compatible with selective read/write operations as the back gate was pulsed. More recently, by pulsing only the device gate and drain, Okhonin et al. [3-5] and Ohsawa et al. [6-8] developed the technology necessary to do the selective write/read operations required in a RAM arrangement. While some of the initial FB memories used complex "poly-Si pillars" [6], more recent cells are based mainly on standard SOI process [3-5, 8].

2. Operating principles

The memory technology proposed in [3-8] relies on the mechanism of impact ionization to write the "1" state and on forward biasing the body/drain junction to write the "0" state. Both states are written by biasing only the gate and drain terminals. In all write operations, the transistor is in its ON state, consuming therefore power. Such writing mechanisms give memory windows of 5 to 10 μA/μm. Pulsing the device gate or drain in a memory matrix can lead to memory disturb and no much data has yet been reported on cell disturb. It is also possible to exploit alternate writing mechanisms for the FB memory cell that allow low power operation, and larger memory windows.

3. Experimental data

The Fig.1 illustrates the current flowing through a cell with standard write/read operations, as published in [3-8]. As can be seen, writing a "1" or "0" state consumes 50μA/μm or 500μA/μm, and a memory window of 10μA/μm is typically obtained for 0.13 μm devices. To write a "1" while keeping the transistor in its OFF state, we can to use band to band tunneling. By applying a negative gate and a positive drain voltage, holes are created in the FB and a "1" state is generated (Fig.2). The writing speed can be adjusted by the Vgd potential. To write a "0" state while keeping the device OFF, we can use a combination of negative gate and drain voltages. The Fig.3 illustrates the current flowing through a cell with low power write/read operations. As can be seen, no current flows through the cell during data writing (the transistor is OFF) and a much larger memory window of 40μA/μm is obtained. The improvement of the memory window comes from the fact that when writing a "1" state by band to band tunneling, the FB capacitance is higher. Even larger programming windows can be obtained by depleting completely the body volume during the "0" write operation. This is demonstrated in Fig.4 by using a recombination mechanism to remove completely the body holes. A memory window of 80μA/μm is achieved.

In our previous studies [3-5], we reported data retention under reading conditions, i.e. while applying a small gate and drain bias on the cell. Fig.5 shows that a much better retention time is obtained by measuring the cell under real holding conditions. A typical retention distribution at 110°C is shown in Fig.6. The retention time is defined as the time giving a 50% charge loss. These retention conditions can be referred to as "static", while in reality the cell switches constantly from holding to "dynamic" conditions where pulses can be applied on the cell gate or drain. Fig.7 shows data retention for pulses applied on the cell drain. As can be seen, the data is not affected unless a few thousand pulses are applied. Above this value, the data loss is due to the cumulated effect of impact ionization in the sub threshold regime. Similarly, Fig.8 shows data retention for pulses applied on the cell gate. In this case, after a few hundred pulses, the data is seriously degraded. This gate disturb degradation is due to charge pumping [9] or carrier recombination at the Si/SiO_2 interface (Fig.9). This gate disturb behavior is however much better than in standard 1T/1C DRAMs, where a single pulse on the gate induces a data loss (destructive read).

3. Experimental data

In this paper we presented a review of FB RAM memory operation extended to new low power writing mechanisms. We also presented first results on data disturb and showed evidence of a charge pumping related gate disturb.

References

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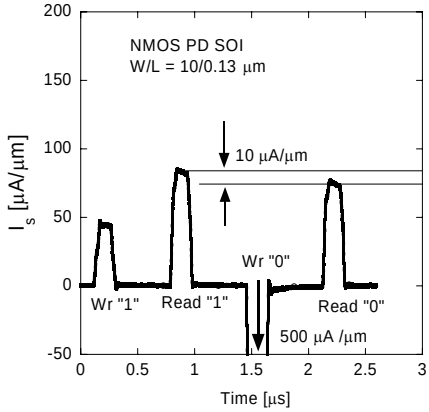

Fig. 1: Write and read currents and programming window for a standard operation of the capacitor less RAM cell.

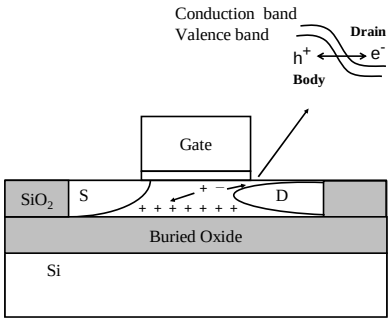

Fig. 2: Schematic illustration of writing a "1" data state by band to band tunneling.

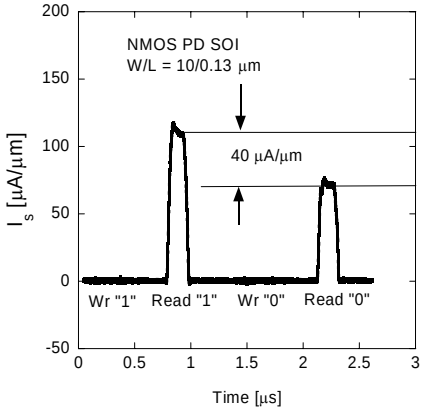

Fig. 3: Write, read currents & programming window for a low power operation of the capacitor less RAM cell.

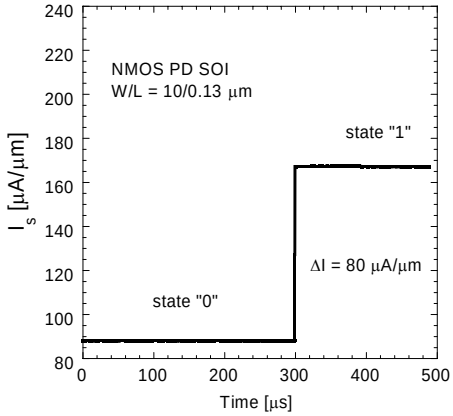

Fig. 4: Maximum memory window by fully depleting the device FB.

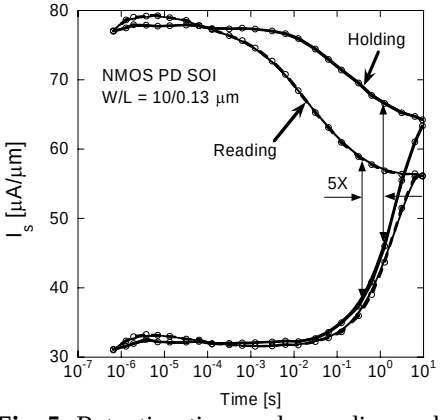

Fig. 5: Retention time under reading and holding conditions.

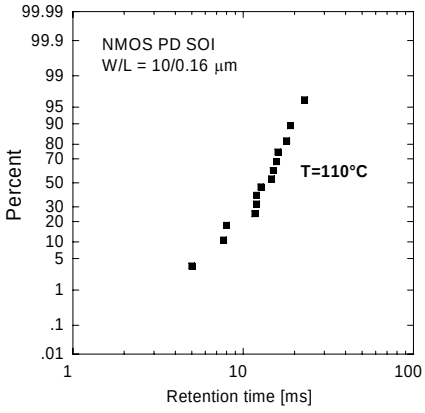

Fig. 6: Retention distribution at 110°C for a typical cell.

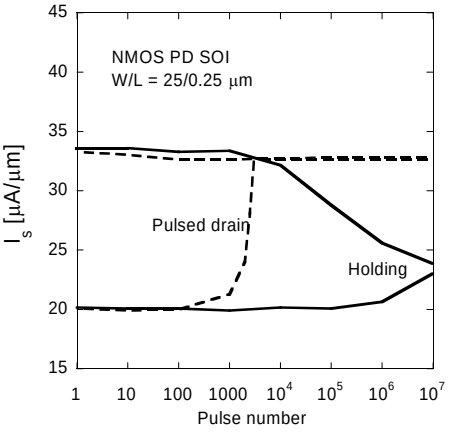

Fig. 7: Data retention under pulsed drain conditions.

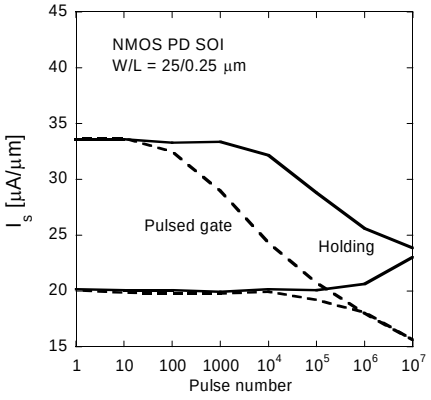

Fig. 8: Data retention under pulsed gate conditions.

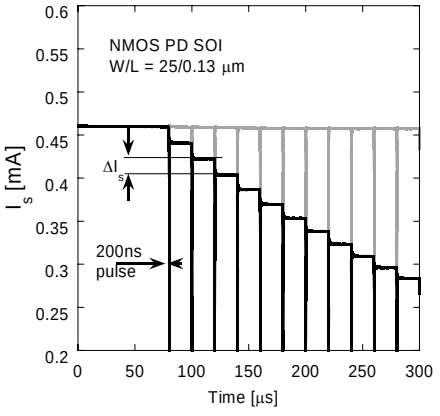

Fig. 9: Effect of gate pulses inducing charge pumping at the Si/SiO_2 interface on the device current.