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A 90nm-node SOI Technology for RF Applications

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1.Introduction

The SOI technology is expected to be one of the candidates for 40Gbps optical network devices and low power 10Gbps devices. It is important to research and eliminate the structural factors that prevent high-frequency operation.

In this paper, we indicate the necessity of the body-tied SOI MOSFET from circuit simulation and analyze test element group NMOS of the normal gate structure with the Partial Trench Isolation (PTI)[8], the T-gate and H-gate structures. We derive the superiority of the PTI structure that has also low input capacitance at the high-frequency operation. We evaluated the high-frequency characteristics of RF-NMOS, varactor, and inductor that fabricated using 90nm-node SOI technology and adopted the PTI process. The NMOS achieves high performance f_{max}=193GHz at V_d=1V. The varactor has quality factor of 27-71 at 5GHz, and 14-60 at 10GHz. The inductors are indicated 40GHz operation by the pattern layout optimization.

2. Transistor Structure Analysis

Our group reported that the 10-GHz circuit simulation applied the SOI transistor with high body resistance showed the large jitter in SSDM2003 [5]. We further simulated the similar circuit in the both cases of the body floating and the body tied. Fig.1 shows the circuit schematics and the simulation results. The input buffer circuit has 8-stage configuration. The output waveforms are generated from 127-bit PRBS input and overlaid in every 1.5 period. The tied body is essential from the results that the jitter of the body floating condition is 10 times larger than that of the body-tied condition.

We evaluated three types of body-tied MOSFETs which compose unit layout shown in Fig.2; (a) Normal gate with PTI, (b) T-gate whose one end of the active area passes under the gate, (c) H-gate whose both ends of the active area pass under the gate. It has been reported that both T-gate and H-gate are available to tie the body in the Full Trench Isolation (FTI). The PTI is the isolation structure that the SOI layer remains under the isolation oxide, and the body region is connected to the body contact region through this SOI layer. Fig.3 shows the cross sections of the Normal gate with PTI and the H-gate with FTI for channel-body contact direction. In the case of the FTI, the active area passes under the gate, so it is considered that the cross region has a large parasitic capacitance which is a disadvantage for high-frequency operation.

Fig.4 shows the gate voltage dependence of the cut-off frequency f_T for three types of NMOSs at Vd=1V. As the gate voltage increases, the f_T difference between the Normal gate and the T/H-gate are increases. In order to analyze this phenomenon, we have derived input capacitance C_{in} from Y-parameters by equation (1)[9]. In general f_T is expressed in equation (2); where C_{gs} is a gate-source capacitance, C_{gd} is a gate-drain capacitance, and sum of C_{gs} and C_{gd} is considered to equal to C_{in}. Fig.5 shows the correspondence between the f_T and the C_{in} of the fabricated NMOS and implies good agreement with the equation.

$$C_{in} = -1/\mathrm{imag}(1/y_{11})/\omega \quad (1)$$

$$f_T = g_m/\{2\pi(C_{gs}+C_{gd})\} \quad (2)$$

3. Discussions

Fig.6 shows the C_{in} dependence on the gate voltage Vg of the three types of transistor presented in Fig.2 at 45GHz. The Vg dependence of the C_{in} for the T-gate and the H-gate are quite larger than that for the Normal gate. The gate area ratio of the each transistor is S_{Norm} : $S_{T\text{-}gate}$: $S_{H\text{-}gate}$ = 1 : 3.8 : 6.5, but this ratio is rather different from the C_{in} ratio of the each transistor. As we calculate the gate capacitance with the gate area and gate oxide thickness, the C_{in} of the Normal gate is comparable, and that of the T-gate and the H-gate are very small. Most of all carriers are supplied by only the source N+ doped layer in the condition of the drain bias 1V. The carriers move by diffusion from the source to the body contact since the body potential equals to the source potential. Their diffusion length is calculated about 0.13μm at 45GHz. If it is assumed that only the carriers are able to follow within 0.13μm from the source region, the ratio of the effective gate area, which affects to a parasitic capacitance, becomes S_{Norm} : $S_{T\text{-}gate}$: $S_{H\text{-}gate}$ = 1 : 2.0 : 3.0. This ratio is rather close to the derived C_{in} ratio, and another reason of the discrepancy is considered to be due to the fixed parasitic capacitances such as the gate overlap capacitance.

4. Integration

A. Process Technology

The normal gate with FTI has a disadvantage on the jitter compared with T/H-gate, and even the T/H-gate layout still has large C_{in} at high frequency as summarized in Table 1. The PTI structure meets the both, so we adopted PTI structure for the 90nm-node SOI process. The key technologies are SOI wafer with high resistance support substrate (more than 1KΩ–cm), 1.8nm-thick gate oxide, Co salicide, Cu and Low-K BEOL.

B. RF-NMOS and Passive Elements

Fig.7 shows the frequency dependence of unilateral gain, $|h21|^2$, MAG/MSG for the NMOS with 65nm gate length at Vd=1.0V, Vg=0.7V; f_T=143GHz, f_{max}=193GHz were derived from –6dB/oct extrapolation. Fig.8 shows f_{max} vs. gate length as compared with recent published MOS. With not only shrinking the gate length but also optimizing the gate width, top-level performance is achieved.

Fig. 9 shows C-V characteristics and Q factors at 5/10GHz of the accumulation MOS varactor from –1V to1V. The gate length of the varactor is reduced to 0.1μm in order to decrease the parasitic resistance of the body region, so the Q factor is improved to 27-71 at 5GHz and 14-60 at 10GHz. Fig.10 shows the excellent Q factor compared with the recently reported varactor.

Fig. 11 shows the Q factor vs. frequency of the Cu inductors with several inductances formed of 1.3μm-thick top Cu layer. The Q factor of the 10μm-wide inductor was around 20 at 10-20GHz. The narrow 3μm-wide inductor reduced the parasitic capacitance, and the Q factor of more than 30 was reached at 40GHz.

4. Conclusion

We demonstrated the superiority of the PTI structure from the high-frequency operation analysis and adopted this process for the 90nm-node SOI technology. The NMOS achieved high performance f_{max}=193GHz at V_d=1V. The varactor had quality factor of 27-71 at 5GHz, and 14-60 at 10GHz. The inductors were indicated 40GHz operation by the pattern layout optimization.

References

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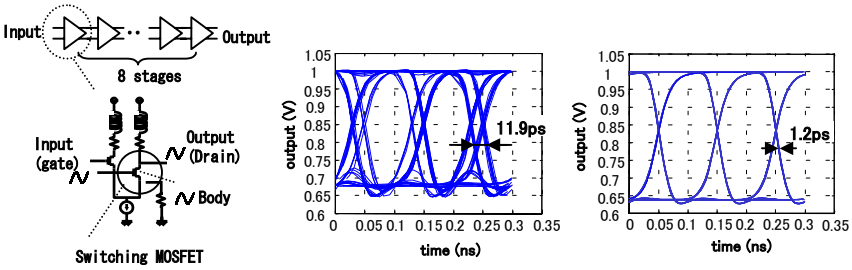
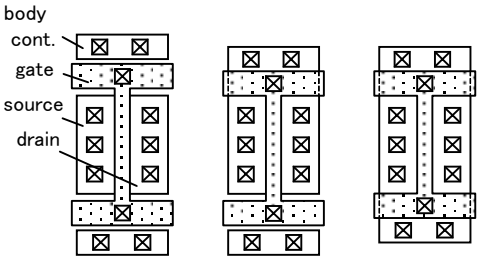


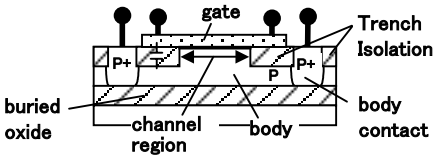
(a) circuit schematics (b) body floating (c) body-tied

Fig.1 Input buffer circuit simulation: the simulated jitter is 11.9ps (body floating) and 1.2ps (body-tied); (a)circuit schematics, (b) wave form at the body floating condition, (c) wave form at the body-tied condition.

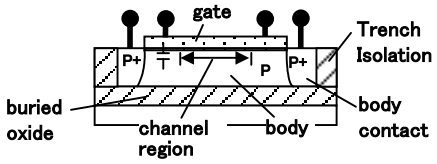


(a)Normal gate with PTI (b)T-gate (c)H-gate

Fig.2 Layout of transistor unit; (a) Normal gate with Partial Trench Isolation (PTI), (b) T-gate, (c) H-gate.



(a) Partial Trench Isolation (PTI)



(b) Full Trench Isolation (FTI)

Fig.3 Cross section of transistor for channel - body contact direction; (a) Partial Trench Isolation, (b) Full Trench Isolation.

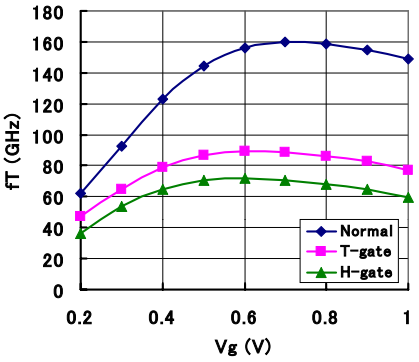


Fig.4 Vg dependence of fT for the 3 types of transistors.

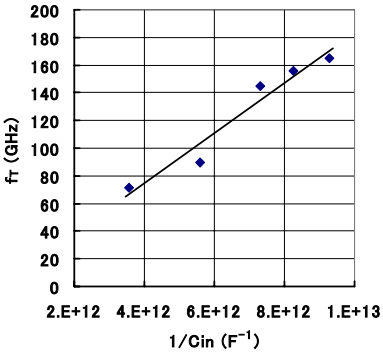


Fig.5 fT vs. input capacitance Cin for the NMOS with the same gate length.

Table.1 Comparison of transistor structure and layout

structure	FTI		PTI
layout	Normal	H/T-type	Normal
jitter	poor (body floating)	good	good
f_T	good	poor (large C_{in})	good

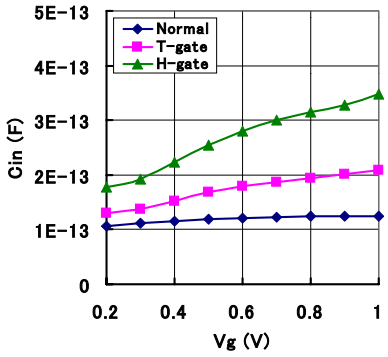


Fig.6 Input capacitance of 3 types of transistors derived from Y-parameter at 45GHz.

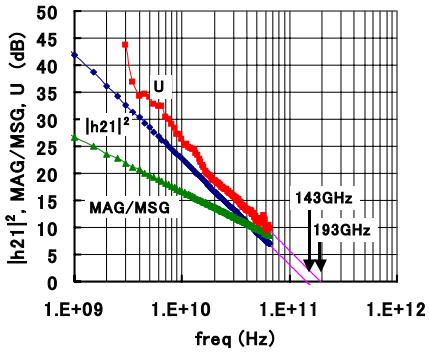


Fig.7 Frequency response of unilateral gain, $|h21|^2$, MAG/MSG of NMOS (Lg=65nm).

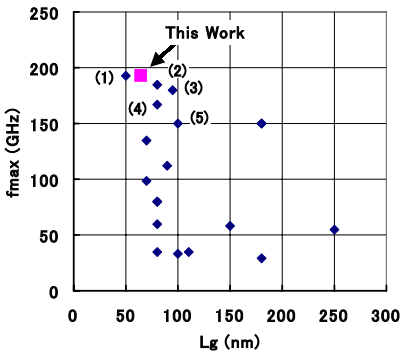


Fig.8 fmax vs.gate length compared with recent published NMOS.

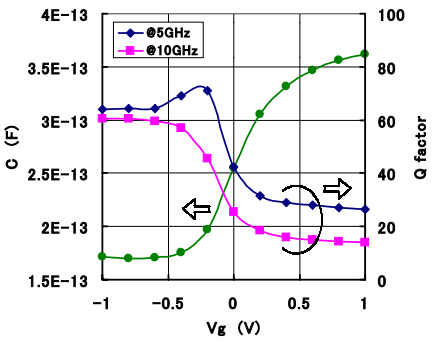


Fig.9 Capacitance and Q factor of the accumulation MOS varactor in the Vg range from –1V to 1V (Lg=0.1μm).

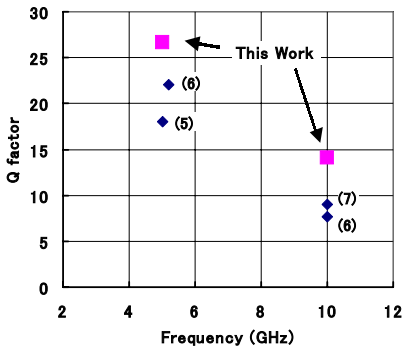


Fig.10 Q factor of the varactor vs. operation frequency compared with recent published varactor.

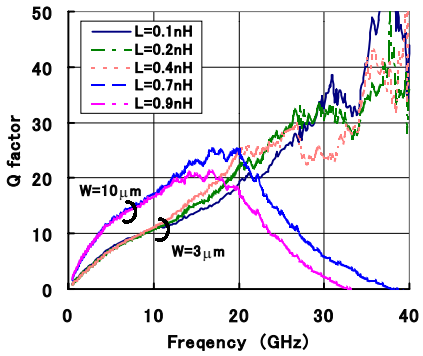


Fig.11 Q factor vs. frequency characteristics of the several inductance of spiral inductors.