# Suppression of Self-Heating in Hybrid Trench Isolated SOI MOSFETs

# with Poly-Si plug and W plug

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## 1. Introduction

## 4. Proposal of PTI with poly-Si plug and W plug

Recently, high-performance and low-power silicon-on -insulator (SOI) device for a system on a chip (SOC) including high-frequency analog and digital circuits is widely investigated. However, the drive current degradation due to self-heating, which is peculiar to SOI devices, is an issue in SOI LSI's. The self-heating causes unstable operation for the high-frequency analog circuits, such as operation frequency modulation due to the reference voltage shift in bias circuits [1]. Moreover, when an analog/digital integrated circuit is considered, there is a possibility that the temperature rise by self-heating of an analog circuit reduces the performance of a digital circuit.

We already reported the distinct validity of the hybrid trench isolation (HTI) structure [2], [3]. In this paper, we propose the HTI with cooling plug structure for the suppression of the self-heating. The self-heating of MOSFETs was monitored by the measurement of gate resistance of the MOSFETs [4]. Device simulation for temperature distribution around the MOSFET was performed for analysis of the measured data. It is predicted that the structure with poly-Si plug in buried oxide and W plug in the partial trench isolation (PTI) is an effective method for reducing of device temperature for the first time.

# 2. Experiment and Results

The device temperature is estimated by temperature dependence of gate resistance [4]. Then, we obtained device temperature as a function of the device power. Fig.1 shows the layout of test structure. MOSFET A (Tr. A) is turned on and MOSFET B (Tr. B) is turned off. Therefore, temperature of Tr. A rises owing to the self-heating. A cross section of the test structure is shown in Fig. 2. The gate oxide thickness is 2.0 nm, and the L/W are 0.2  $\mu$ m/10  $\mu$ m. Gate to gate distance is 0.5  $\mu$ m and contact plug diameter is 0.2  $\mu$ m. SOI layer thickness is 130nm, and buried oxide (BOX) thicknesses are 400 nm and 142 nm.

Fig. 3 shows the measured temperature of Tr. A as a function of the device power of Tr. A for SOI and bulk MOSFETs. As the device power increases, the device temperature rises. The amount of device temperature rise becomes large as the BOX thickness increases because of the large thermal resistance of the oxide layer. Fig. 4 shows the temperature of Trs. A and B as a function of the power of Tr. A. As the power of Tr. A increases, the temperature of Tr. B also rises because of the heat conduction through SOI layer between the Trs. A and B. Fig. 5 shows the thermal resistance of SOI and bulk MOSFETs. Thermal resistance of Tr. B is half of that of the Tr. A.

### 3. Simulation and analysis

Comparison of a simulation and the measured data are shown in Fig. 6. This simulation consists of three sorts, Si, SiO<sub>2</sub>, and W, and those thermal conductivities are 150 W/mK, 1.4 W/mK, and 177 W/mK, respectively (Fig. 6(a)). Both of the temperature at the top of a contact plug and the bottom surface of a silicon substrate are 300 K. The temperature of SOI MOSFET is higher than that of BULK MOSFET (Fig. 6(b)), because thermal resistance of BOX is higher than that of silicon substrate. Fig. 6(c) shows the SOI device temperature as a function of the BOX thickness. The measured data shows a very good agreement with simulation.

In the previous paragraph, we discussed the heat conduction in only SOI layer between MOSFETs. Then, in this paragraph, heat conduction in isolation regions is also studied because optimization of the isolation structure is important to suppress the self-heating. The mechanism of the heat conduction of the general full trench isolation (FTI) and the PTI are shown in Fig. 7(a). In the case of the FTI SOI MOSFET, increased temperature by self-heating could not be reduced because the heat conduction is limited by the buried oxide and the isolation oxide. Therefore, the PTI is a suitable structure for the suppression of the self-heating. However, it is anxiety that temperature rise of the around device is caused by the heat conduction through the SOI layer under the isolation oxide. Then, we propose a new isolation structure where a temperature rising due to self-heating can be reduced. Fig. 7(b) shows the concept of the new isolation structure which is the PTI structure with cooling plugs. These plugs are consists of poly-Si plug in buried oxide and W plug in partial isolation oxide. Since they have high thermal conductivity, the PTI with plug structure is quite effective for heat diffusion. We can show the usefulness of proposed structure by the simulation.

Fig. 8(a) shows the temperature distributions simulated for FTI and PTI SOI MOSFETs. The temperature of the Tr. A for FTI structure is higher than that of PTI, because the isolation oxide between the Trs. A and B protects the heat diffusion. On the contrary, temperature of the Tr. B of PTI is higher than that of FTI. The temperature rise around Tr. B of PTI is due to the heat diffusion through the SOI layer under the isolation oxide.

Furthermore, Fig. 8(a) also shows temperature distributions of the proposed structure. The temperature of Trs. A and B with the PTI and plug structure are lower than that of the PTI structure. Heat from the Tr. A conducts through the both of the plugs. While temperature of Tr. B with the PTI and plug is almost the same that the FTI MOSFET, temperature of Tr. A decreases drastically compared to that with FTI (Fig. 8(b)). These plugs can be fabricated on the device isolation regions, therefore, there is no area penalty. Moreover, poly-Si plug can be separated from source/drain regions. Therefore, features of SOI MOSFETs such as low parasitic capacitance and body tied structure can be kept.

### 5. Conclusion

Temperature rise due to self-heating was investigated for the operated MOSFET and the around MOSFET with several buried oxide thickness. Device thermal resistance of the around MOSFET is half of that in the operated MOSFET. The measured results was proved and analyzed by the device simulation. The PTI SOI MOSFET is the suitable structure for the heat suppression rather than FTI SOI MOSFET because the SOI layer under the PTI assists the heat conduction. Moreover, the effect of the heat reduction of PTI with plug structure is proved by the device simulation. The HTI structure with the cooling plugs enables to manage the self-heating issue.

### References

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Fig. 1 Plane view of the experimental test structure layout.





(c)

- Fig. 6 Comparison of measurement results and simulated results. (a) Simulated structure.
  - (Top of W and bottom of Si substrate at 300 K.)
- (b) Simulated temperature distributions of SOI (BOX=400nm) and BULK MOSFETs.
- (c) Device temperature of Trs. A and B vs BOX thickness at Tr. A operation.



Fig. 2 Cross sectional view of test structure of SOI MOSFET.



Fig. 4 Measured device temperature of Trs. A and B as a function of power of Tr. A. ( Tr. A: operated MOSFET, Tr. B: nearness MOSFET )





Fig. 3 Measured device temperature of Tr. A as a function of the SOI and BULK.



Fig. 5 Device thermal resistance of both Trs. A and B of SOI and bulk at Tr. A operation.



- Fig. 7 The mechanism of the heat conduction of the several isolation structures.
- (a) Full trench isolation (FTI) and Partial trench isolation (PTI).
- (b) Proposed isolation structure (PTI with the cooling plugs).



Fig. 8 Simulated temperature distribution of proposed structure (FTI, PTI, PTI + plug).

(a) Temperature distributions of three types of structures.

(b) Device temperature of Trs. A and B for several isolation structure at Tr. A operation.