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Floating Body Accelerated Oxide Breakdown Progression in Ultra-Thin Oxide SOI pMOSFETs

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1. Abstract

Enhanced oxide breakdown progression in ultra-thin oxide (1.4nm) SOI pMOS is observed, as compared to bulk devices. The enhanced progression is attributed to the increase of hole stress current resulting from breakdown induced channel carrier heating in a floating-body configuration. Numerical analysis of hole tunneling current and hot carrier luminescence measurement are performed to support the proposed theory.

Keywords: breakdown progression, SOI pMOS, carrier temperature, body potential.

2. Introduction

It has been reported that oxide breakdown (BD) behavior in ultra-thin oxides is quite different from that in thicker oxides [1-3]. Fig. 1 shows that oxide BD in a 1.4nm oxide pMOS is evolved in a progressive way and the oxide leakage current increases slowly with stress time. Previous study has shown that a small increase in gate leakage due to oxide BD is considered to be nondestructive for circuit operation [4]. The criterion for oxide failure is thus determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate.

In this work, we observe an enhanced BD progression rate in 1.4nm oxide PD SOI pMOS, as compared to bulk devices (Fig. 2). The Weibull distribution of oxide t_{BD} and t_{fail} for SOI and bulk pMOS is plotted in Fig. 3. The gate stress voltage is –2.9V. t_{BD} and t_{fail} are defined as 50% and 15X increase in gate current, respectively. Although SOI and bulk devices exhibit the same time-to-breakdown ($t_{BD)}$, the SOI pMOS apparently has a shorter time-to-failure ($t_{fail)}$.

3. Mechanism for Floating-body Enhanced BD Progression

The floating body configuration of SOI devices will result in a small forward body voltage due to various body charging processes. The SOI samples were fabricated with an additional body contact to facilitate the measurement of body potential and current. To analyze the polarity of gate stress current, a charge separation measurement is performed (Fig. 4(a)). Fig. 4(b) shows that the dominant stress current changes from electron current (I_b) to hole current (I_{sd}) after t_{BD}. *More interestingly, unlike I_b and I_{sd} in a fresh device, the post-t_{BD} hole current exhibits significant body bias (V_b) dependence (Fig. 5).* This V_b dependence is more distinguished at a smaller gate bias (Fig. 6). Fig. 7 shows the range of stress gate bias where hole current is dominant. Because hole stress current dominates during BD evolution and it increases with a forward body bias, the enhanced BD progression due to the floating body configuration in SOI can be understood. Fig. 8 compares the time-to-failure in SOI and bulk pMOS. Accelerated BD progression is noticed in SOI samples. This trend is more apparent at lower stress gate biases. The measured result is consistent with the V_b dependence in Fig. 6.

4. BD Caused Carrier Heating and V_b Dependence

Since the post-t_{BD} electron current does not exhibit V_b dependence (Fig. 5), *the possibility that the V_b dependence of the post-t_{BD} I_{sd} is caused by the variation of effective gate-to-channel voltage [2] resulting from V_b modulated channel resistance is excluded.* Otherwise, the post-t_{BD} I_b should have similar V_b effect. Moreover, substrate impact ionization and NBTI effects are also excluded because the trend of the V_b dependence is opposite.

Fig. 9 shows the measured spectral distribution of hot carrier light emission in a post-t_{BD} pMOS. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300K (Fig. 9(b)). The possible explanation for the rise of carrier temperature is that high-dissipated energy, released by valence electrons from the gate through the BD path, will locally produce a temperature rise of carriers in the channel [5]. In order to show that an elevated hole temperature may account for the observed V_b dependence, we calculate the hole tunneling current with hole temperature at 300K and 1300K through the Tsu-Esaki formula [6],

$$I_{sd} = qm^*\left(\frac{1}{2\pi^2\hbar^3}\right)k_BT\sum_n D_n\{\ln(1+\exp((E_n-E_f)/k_BT))) - \ln(1+\exp((E_n-E_{f'})/(k_BT)))\} \quad (1)$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the n-th sub-band. Other variables have their usual definitions. The detail of the calculation can be found in our earlier publication [3]. *It should be emphasized that it is not our intention here* to model trap-assisted charge transport in the BD path. Instead, our purpose is to investigate the effect of hole temperature on hole distribution in sub-bands and corresponding V_b effect on hole tunneling current. Our simulation (Fig. 10) clearly reveals that the V_b dependence of the hole tunneling current indeed increases with hole temperature. The trend is similar to the measured V_b dependence in Fig. 6. To explain the temperature effect on the V_b dependence in more detail, the distribution of inversion holes in the lowest three sub-bands is given in Table. 1. At T=300K, channel holes mostly reside in the first sub-band no matter of V_b. At T=1300K, a large part of holes are thermally excited to higher sub-bands at a forward body voltage (-0.3V), where the oxide tunneling probability is larger. Thus, a much larger hole tunneling current is obtained at V_b= -0.3V.

5. Conclusion

In ultra-thin oxide SOI pMOS, breakdown progression is aggravated by a forward body bias. A larger post-t_{BD} gate current is observed in SOI devices (Figs. 2&5). The V_b accelerated BD progression has large impact on the failure time of SOI and DTMOS devices.

References

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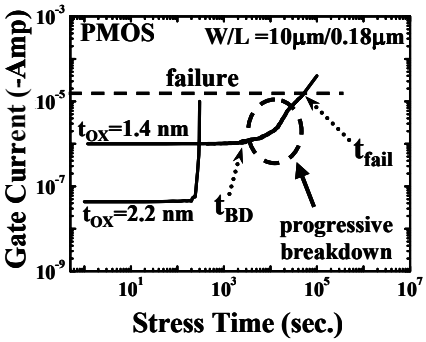

Fig. 1 Comparison of breakdown behavior in a 1.4nm oxide pMOS and in a 2.2nm oxide pMOS. The stress gate voltage is –2.6V for the 1.4nm oxide and –3.9V for the 2.2nm oxide. t_{BD} denotes the onset of oxide breakdown.

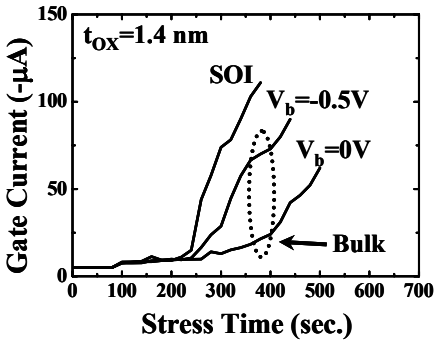

Fig. 2 Oxide breakdown progression in bulk and SOI pMOS. Stress V_g=-2.9V at T=125C.

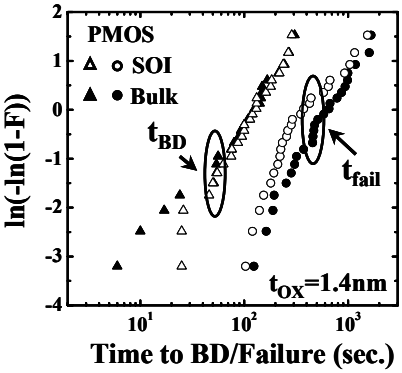

Fig. 3 Weibull plots of t_{BD} and t_{fail} distribution for 1.4nm oxide devices.

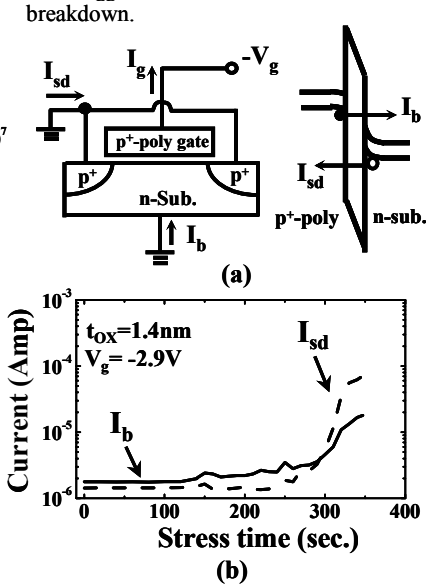

Fig. 4(a)Illustration of current flow in a pMOS at a negative gate bias. I_b (I_{sd}) denotes electron (hole) stress current. (b)Electron and hole current components versus stress time.

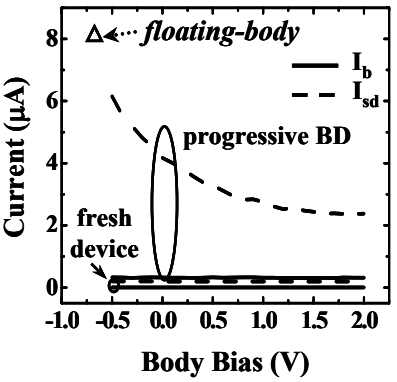

Fig. 5 The dependence of electron current and hole current on body bias at Vg=-1.5V. Hole current during progressive BD in a floating-body configuration is indicated.

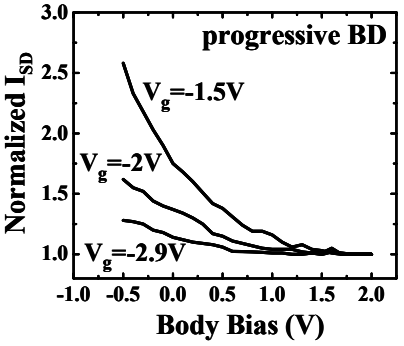

Fig. 6 Body bias dependence of hole current at various gate biases. I_{sd} is normalized to its value at V_b=2V.

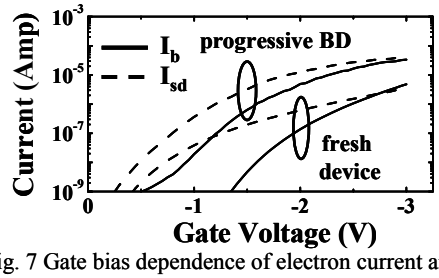

Fig. 7 Gate bias dependence of electron current and hole current in a fresh pMOS and during progressive BD.

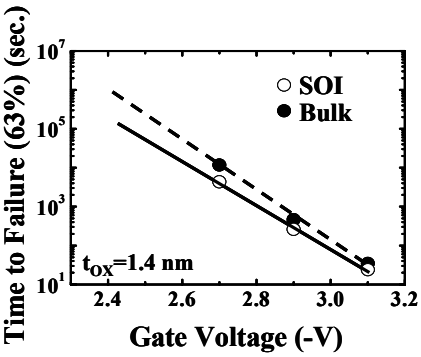

Fig. 8 t_{fail} (63%) vs. stress gate bias for SOI and bulk pMOS devices.

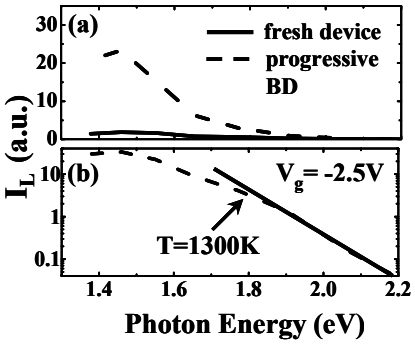

Fig. 9 (a)Spectral distribution of light emission in a 1.4nm oxide pMOS at V_g=-2.5V. (b)The extracted carrier temperature is around 1300K.

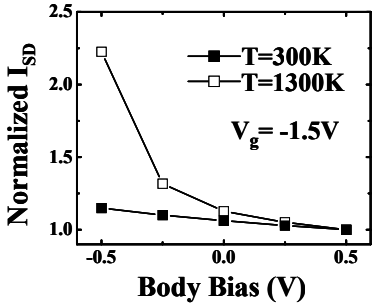

Fig. 10 Simulated body bias effect on hole tunneling current in a 1.4nm oxide pMOS. I_{sd} is normalized to its value at V_b=0.5V.

Table 1 Calculated distribution of channel holes in the lowest three sub-bands.

cond. / sub-band	channel hole dist. (%)			
	300K		1300K	
	V_b=-0.3	V_b=2	V_b=-0.3	V_b=2
1st	98	99.9	62.7	81.3
2nd	1.9	0.1	13.8	13.1
3rd	0.1	0	6	3.5