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Ultra-Shallow Junction Formation using Novel Plasma Doping Technology beyond 50 nm MOS Devices

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1. Introduction

Recently, as strenuous efforts are being focused on further scaling of MOSFETs into sub-100 nm regime, the short channel effects (SCE) become a serious problem. The ultra-shallow S/D junction formation technologies with abrupt doping profile are required to suppress SCE in the future silicon MOSFETs of sub-100 nm gate length regime. Low energy ion implantation or plasma based ion implantation is now being considered as a promising technique for shallow junction formation and large area doping in CMOS technology [1,2]. In this paper, we report a novel elevated temperature plasma doping (ET-PLAD) technique for nano-scale SOI n-MOSFETs.

2. Experimental

SOI n-MOSFETs were fabricated on p-type (100) UNIBOND SOI wafers with a 30 nm top silicon layer and a 200 nm buried oxide. The active region was defined in the top silicon layer using a combination of electron-beam lithography (EBL) and photolithography to produce a narrow channel with a 30 nm width. After gate oxidation of 3 nm, a phosphorus doped polysilicon film with 100 nm thickness was deposited as a gate electrode. The EBL technique using HSQ resist was also used to produce the 50 nm gate line. We used the ET-PLAD to form the SDE without additional thermal processes. The ET-PLAD process was carried out by plasma doping system using the 1 % diluted PH_3 in He gas. Simultaneously, H_2 gas was introduced to stabilize the plasma and for the hydrogenation treatment. Phosphorus ions were implanted with the 0.5-5 kV acceleration voltage ranges. The substrate temperature of PLAD process was controlled in the range of 27-230°C. Also, n^+-p diodes and nano-scale SOI n-MOSFETs with 50 nm gate length and 30 nm channel width were fabricated by ET-PLAD.

3. Results and discussions

Fig. 1 shows SIMS depth profile of phosphorus after PLAD and RTA. In case of the conventional elevated temperature plasma doping (RT-PLAD), the junction depth Xj was significantly increased after the RTA activation annealing process. On the hand, the Xj was not changed by the ET-PLAD process at 230°C. Fig. 2 shows sheet resistance as a function of PLAD temperature. A low sheet resistance (Rs) of 920Ω/□ was obtained by ET-PLAD at 230°C without additional activation annealing. The laterally abrupt SDE junctions can be obtained, because the temperature of PLAD is too low for dopant to diffuse as shown in Fig. 1. The behaviors of Rs are related to the crystalline defects as shown in Fig. 3. The PLAD at higher process temperature is more effective for reduction of crystalline defects, because the satellite peak of Raman spectra decreased with increasing PLAD temperature [3]. Fig. 4 shows the Crossectional TEM images of (a) RT-PLAD and (b) ET-PLAD samples. These TEM images show that the crystal defects generated by the RT-PLAD could be suppressed by using the ET-PLAD process, which showed a good aggrement with the Raman analysis. Fig. 5 shows subthreshold characteristics for the SOI n-MOSFETs (L_g=1 um, W_{ch}=2 um) fabricated by ET-PLAD process. Although, the activation annealing was not carried out, the SOI n-MOSFET showed good operational characteristics. The subthreshold swing of MOSFETs decreased as the PLAD temperature increased; 97 mV/dec for 60°C, 78 mV/dec for 150°C, and 62 mV/dec for 230°C. The electrical characteristics of 100 nm gate length SOI n-MOSFETs are shown in Fig. 6. It is found that the SCE was effectively suppressed by ET-PLAD, because the drain induced barrier lowering (DIBL) was 50mV. Fig. 7 shows the I-V characteristics of multi-channel tri-gate MOSFETs with a gate length of 50 nm fabricated by 230°C ET-PLAD. The inset shows a SEM image of the tri-gate MOSFETs. Although a sidewall spacer was not formed, excellent electrical characteristics, SS=150mV/dec and DIBL=40mV/V, were obtained. Based on these results, we suggest that the ET-PLAD is an effective doping process in sub-50 nm MOSFETs.

4. Conclusions

A novel PLAD technique for ultra-shallow junction formation at elevated temperature has been presented. The elevated temperature PLAD is an excellent process for fabricating the sub-50 nm SOI MOSFET devices. Also, the experimental results suggest that the ET-PLAD is compatible with the high-k gate dielectrics, because the ET-PLAD is sufficiently low- temperature process.

References

[1] Kilho Lee et al., *VLSI Tech. Dig*. (2001) p. 21-22.
[2] D. Lenoble et al., *2nd International Workshop on Junction Technol.* (2001) p.29.
[3] C. Droz et al., *Proc. European Photovoltaic Solar Energy Conf*. (2001) p. 2917.

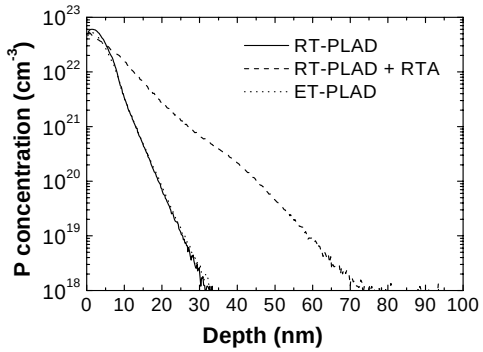


Fig. 1 SIMS depth profiles of phosphorus. RT-PLAD and ET-PLAD were carried out at 27°C and 300°C, respectively. RTA was carried out at 950°C for 30s.

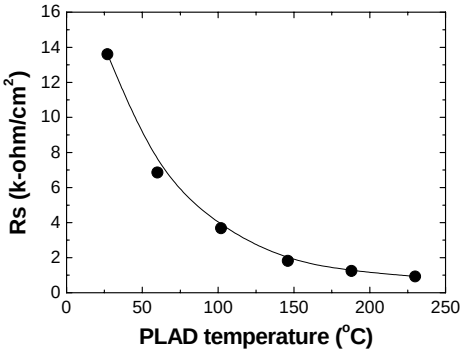


Fig. 2 Sheet resistance (Rs) vs. PLAD temperature.

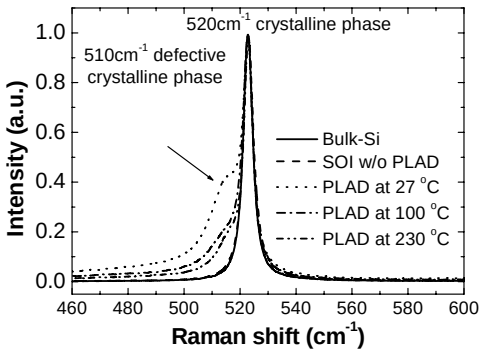


Fig. 3 Raman spectra vs. PLAD temperature.

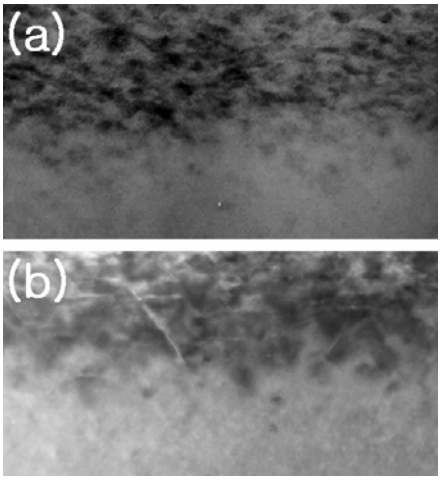


Fig. 4 Crossectional TEM images of (a) RT-PLAD and (b) ET-PLAD samples.

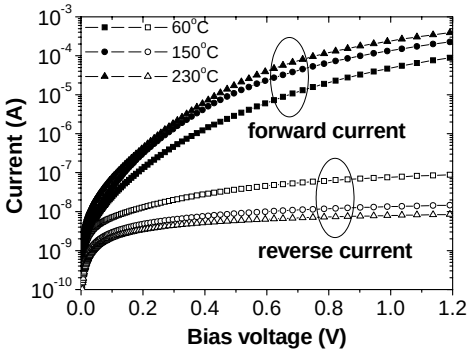


Fig. 5 Current-voltage curves of n^+-p diode fabricated by ET-PLAD.

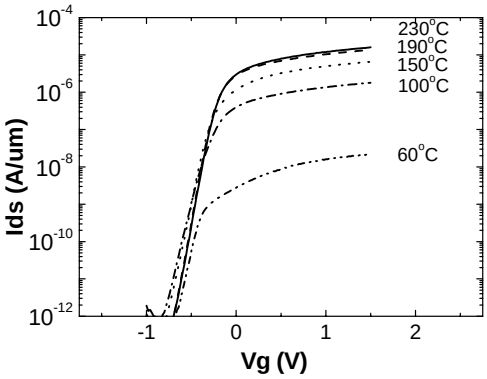
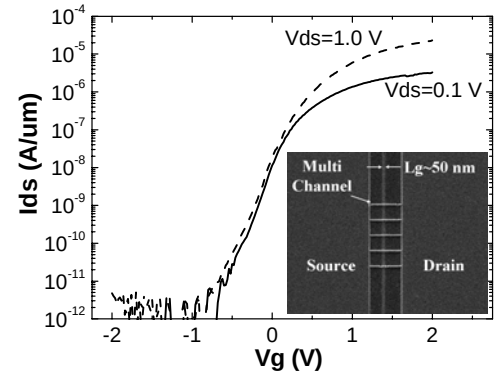


Fig. 6 Subthreshold characteristics of large size SOI n-MOS FETs (L_g=1 um, W_{ch}=2 um) as a function of PLAD temperature.



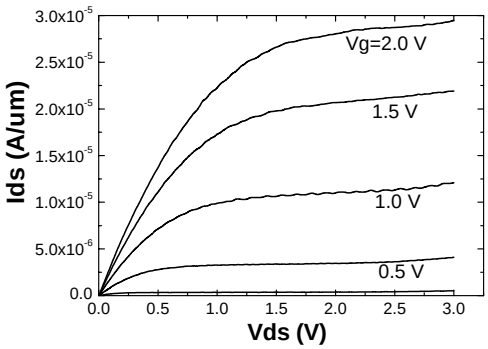


Fig. 7 Current-Voltage characteristics of tri-gate n-MOSFETs (L_g=50 nm, W_{ch}=30 nm) fabricated by ET-PLAD (230°C). Inset shows a SEM image of multi-channel tri-gate n-MOSFETs.