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SOI Transistor/Power Scaling and Scaling-Strengthened Strain

Fu-Liang Yang, Hou-Yu Chen, and Chang-Yun Chang
Taiwan Semiconductor Manufacturing Company, No. 8, Li-Hsin Rd. 6, Hsinchu Science Park, Hsin-Chu, Taiwan, R.O.C.
Phone: 886-3-6665152, E-mail: flyang@tsmc.com

1. Introduction

Silicon on Insulator (SOI) has been well known by its advantages on high performance applications [1]. Recent years scaling ability of SOI is also addressed by several researches [2-3]. Meanwhile, strained silicon has become a critical technique for CMOS scaling. Since active region of SOI device is decoupled from substrate by buried oxide, the channel strain should be more pronounced and sensitive to device features. In this paper, SOI transistor scaling by means of silicon thickness reduction and structure evolution will be reviewed. Furthermore, strain effect in SOI and potential issues will be discussed from transistor scaling viewpoint.

2. SOI Transistor/Power Scaling

Transistor scaling

A large potion of performance gain in SOI technology comes from reduced junction capacitance, and this benefit is more significant in thin body SOI. Moreover, short channel effect can be suppressed by the aid of thin body due to enhanced gate control over whole body region. As a result, SOI transistor scaling usually comes along with the scaling of silicon thickness (T_{si}). Ultra thin body (UTB) SOI would just be the case with ultimately scaled T_{si} (Fig.1a). Sub-10nm gate length device have been demonstrated [4]. Remaining challenges would be the threshold voltage adjustment, source/drain resistance reduction, and silicon film thickness control in manufacturing.

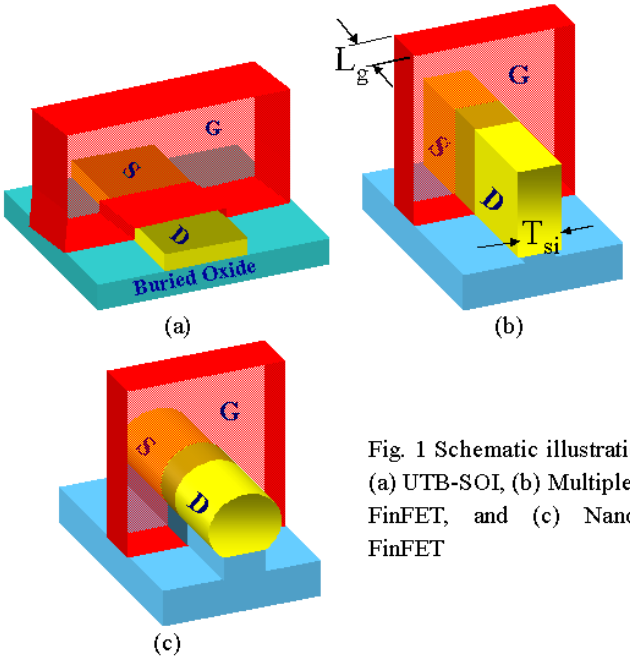

Fig. 1 Schematic illustration of (a) UTB-SOI, (b) Multiple-gate FinFET, and (c) Nanowire FinFET

In recent years, narrow-width multiple-gate SOI devices have been widely proposed [5-7]. Excellent transistor characteristics have been demonstrated with 20nm L_g [7]. In addition, the criteria of T_{si} for full depletion is relaxed and roughly equal to L_g (Fig. 1b). The relaxed body dimension requirement compared with single-gate UTB device will be an advantage for manufacturing. Particularly, newly proposed "Nanowire FinFET" have shown extreme scalablility of multiple gate device, and could further extent T_{si} to $2L_g$ even L_g is only 5nm (Fig. 1c) [8]. Since these narrow transistors have a 3D structure, however, layout and design methodology should be reconsidered. And advanced print technique such as spacer lithography will be very attractive in order to obtain maximum effective channel width in a given layout area [6].

Power scaling

Active power dissipation has become a serious issue for today's VLSI technology since more transistors are integrated into a smaller chip and operating in a higher frequency. Reducing supply voltage surely will alleviate the problem but meanwhile degrade drive current. Although SOI with small parasitic capacitance already have intrinsic benefit to achieve same performance with lower power than its bulk counterpart, however, it is still preferred finding ways to scale supply voltage while maintaining overall performance. Adopting FinFET or FinFET-like device in SOI may probably approach to this goal. It has been reported that FinFET holds a speed advantage over planar SOI on low voltage operation (Fig. 2) [9]. Besides, thicker gate stack thickness in FinFET will greatly reduce gate leakage; hence overall static power dissipation is simultaneously improved.

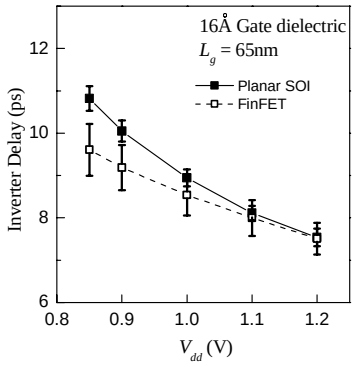

Fig. 2 FinFET shows less speed degradation than planar SOI as supply voltage is scaling.

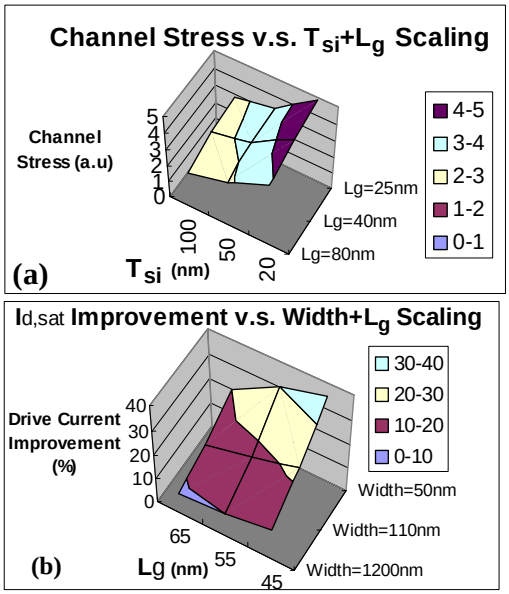

Fig. 3 (a) Channel stress is increased with decreasing T_{si} and L_g. (b) Drive current improvement from channel strain is more significant in small device dimension.

3. Scaling-Strengthened Strain

Enhanced strain in scaled SOI transistor

Strained silicon has been paid much attention for several years to enhance transistor drive current [10-12]. Among several strain techniques, tensile nitride cap layer has been proven as an effective stressor for N-FET with lower cost and defect than biaxial strain [12]. Tensile channel strain is induced by deposited high tensile stress film. Since active silicon region is fully isolated, channel stress cannot be relaxed through silicon substrate underneath buried oxide. This results in a phenomenon that the magnitude of channel stress eventually depends on device aspects (L_g, width, and T_{si}). As shown in Fig. 3 (a), channel stress monotonically increases with scaling silicon thickness (T_{si}) from 100nm to 20nm. Meanwhile, drive current improvement tends to be larger in short-length, narrow-width devices, indicating larger strain in small dimension as shown in Fig. 3(b). The scaling-strengthened strain in SOI transistor is desired since it makes a positive feedback during technology scaling.

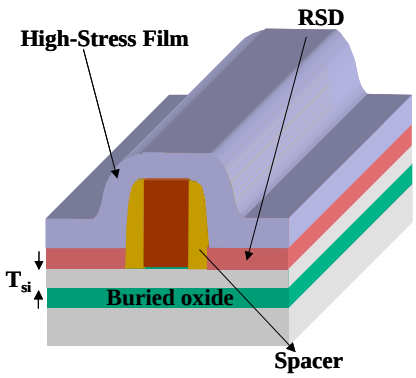

Fig. 4 Raised source/drain (RSD) will increase distance between cap layer (high-stress film) and transistor channel.

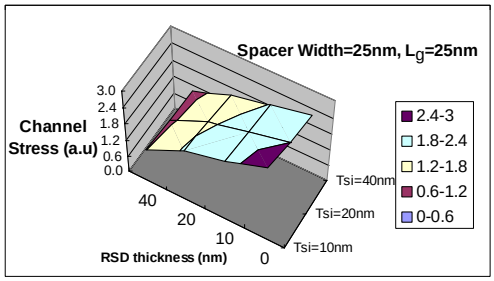

Fig. 5 Channel stress versus different T_{si} and RSD thickness.

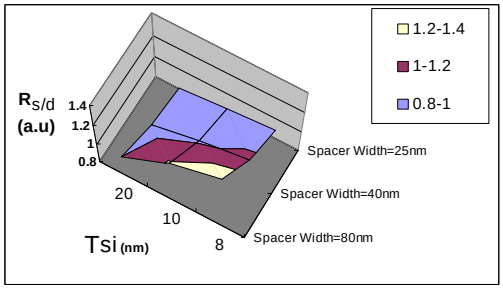

Fig.6 Sheet resistance (Rs/d) versus different T_{si} and spacer width.

Channel stress v.s. source/drain sheet resistance

Continuously scaling T_{si} brings an undesired increment of source/drain sheet resistance (Rs/d). For ultra thin film SOI devices (T_{si} <20nm), raised source/drain (RSD) technique is usually adopted. However, uniaxial channel stress induced by cap layer (high-stress film) may be degraded due to increased distance from stressor to channel as illustrated in Fig. 4. Fig. 5 shows how channel stress varies with different RSD thickness. Simulation predicts a decreasing strain magnitude with increasing RSD thickness. The optimal point between Rs/d and channel strain should be found to maximize drive current. Another solution is to use small spacer to improve source/drain resistance while make T_{si} very thin. Simulation shows Rs/d can be maintained even though T_{si} is scaled from 20nm to 8nm, as long as spacer width is also shrunk from 40nm to 25nm (Fig. 6).

4. Conclusions

SOI transistor scaling will continue with silicon thickness reduction. Multiple gate device with 3D structure could be another candidate for extremely scaled transistor. Strained silicon incorporated with SOI will benefit transistor scaling, yet it may face the tradeoff between sheet resistance and mobility enhancement.

References

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