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Development of SGOI and sSOI for High Volume Manufacturing

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1. Introduction

Engineered substrates [1] are one of the most important innovations of the nanotechnology era. New materials like strained silicon [2-5] and hybrid bonding SOI [6-8] have added new handles to traditional scaling to further improve device and IC performance. It has been shown that strained silicon on insulator (sSOI) [2-4] and strained silicon on relaxed silicon germanium on insulator (SGOI) [2, 5, 9-10] strongly improve the mobility and current drive of NMOS and PMOS devices depending on the Ge content of the SiGe template used to create the strain [5, 11]. In this paper we focus on the strained SOI fabrication resulting from a SiGe 20%Ge template.

2. Substrate Engineering

Substrate Engineering

The potential of engineered substrates is illustrated in figure 1. The power of Smart Cut™ technology [12-14] is that it makes possible to create a fully engineered substrate tailored to the requirements of the application by properly choosing the active layer, the buried dielectric and the base substrate. Starting from an SOI wafer there is an evolution departing from Si (100) as the active layer towards Si (110), strained Si, and even Ge to provide mobility enhancing substrates. The mainstream choice for the buried dielectric is thermal oxide but work is ongoing evaluating the use of deposited dielectrics [14] which also opens the possibility of including buried patterns in the dielectric layer. Lastly, the substrate offers also several options like being high resistivity Si for RF applications, or being non silicon.

SGOI and sSOI

Strained SOI substrates follow an evolutionary path starting from SOI. Depending on the substrate fabrication it will allow for a combination of mobility enhancement features for NMOS as well as for PMOS. For a strained Si film grown on a fully relaxed SiGe (20% Ge) template a biaxial stress level of 1.3 to 1.5 GPa is achieved [2, 9]. This leads to a mobility enhancement of 80% for the NMOS, resulting in an increase of 40% in current drive. If the concentration of Ge is increased up to 40% the same level of mobility enhancement is also achieved for p-channels [5].

The SGOI substrate can be manufactured by layer transfer [2] or by the condensation technique [10]. The SiGe layer serves as a template for the subsequent strained Si epitaxy. The strained Si layer is kept below the critical thickness. The total layer thickness is adjusted by the underlying SiGe layer. Typical values are 300Å for the SiGe and 200Å for the strained Si layer. The SGOI is well suited for a partially depleted IC architecture. For a successful CMOS integration on SGOI, the CMOS thermal budget needs to be carefully adjusted to avoid issues like Ge up diffusion into the strained Si layer creating gate oxide failure, or generation of crystal defects in the sSi layer.

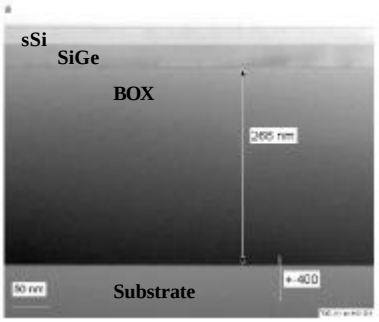

Fig. 1 Example of SGOI, strained si on relaxed SiGe (20% Ge) on insulator. The thickness is adjusted to the device design.

The other type of strained SOI is strained silicon on insulator (sSOI). The strained Si film (sSi) is typically 200Å thick and well suited for a fully depleted CMOS architecture. The advantage of sSOI is that at low V_T, i.e. low channel doping levels, it will maximize the amplification factor of the mobility and current drive of the transistors.

Manufacturing of SGOI and sSOI

The fabrication sequence [2] of sSOI and SGOI is similar to the SOI manufacturing process. Main differences to SOI are the tailored donor wafers with sSi and SiGe epitaxial layers. Further specific steps are the selective removal of SiGe with respect to sSi in the case of sSOI and the final sSi epi for SGOI. The key to a good final quality of the strained SOI is the fabrication of the donor wafer. The Smart Cut technology has been optimized to avoid defect generation during layer transfer. Thus, the crystal quality of strained SOI is directly correlated to the quality of the donor wafer.

A buffer epitaxial layer is use to set the Ge content to the target concentration allowing the SiGe buffer to relax by defect generation. The buffer layer determines the final level of relaxation achieved (>90%). A subsequent SiGe epi step defines the template for the sSi growth. For sSOI fabrication a final sSi epi follows. The top 500nm of the donor wafer is determining for the resulting crystal quality of sSOI and SGOI. Fig. 2 shows the improvement of the starting material in defect density and surface roughness for different epitaxial processes. At present, a threading dislocation density of 10^3-10^4cm^{-2} and an pile-up density of 2-15 cm^{-1} are achieved.

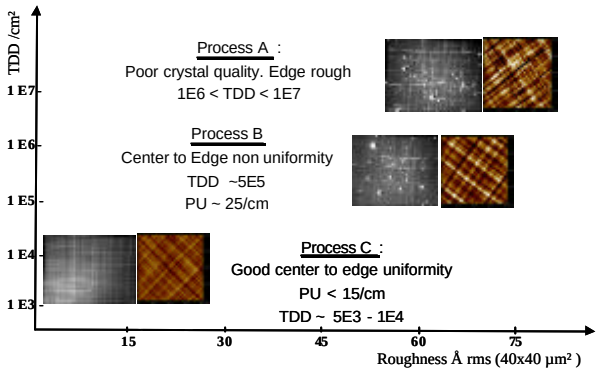

Fig. 2 Donor wafer learning curve in threading dislocation density and surface roughness for different epitaxial processes. Pairs of AFM and Schimmel etch decoration are shown. The white spots on the Schimmel etch micrographs correspond to threading dislocations, the thick highlighted lines to pile-ups. The background soft lines are due to the cross hatch.

The final quality and uniformity of the strained Si film grown on the SiGe template on insulator is coupled to not only to the crystal quality of the SiGe but also the thickness uniformity of the buried oxide and SiGe. In fact the effective sSi epi growth temperature is modulated by the underlying films and its local thickness resulting in sSi thickness variations. The learning curve on sSi thickness variation is shown in Fig. 4. A sigma of 5Å is achieved for a 200Å sSi film with an underlying SiGe of 500Å with a sigma of 13Å. Work continues to eliminate sSi thickness variations.

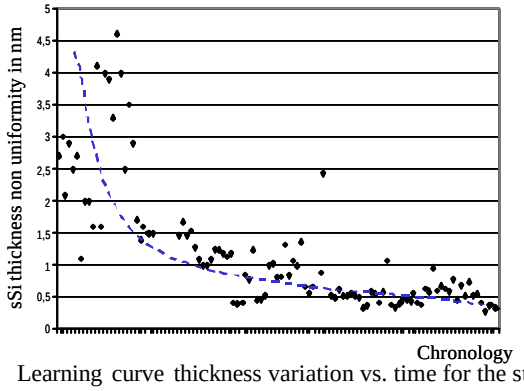

Fig.3 Learning curve thickness variation vs. time for the strained Si final epitaxy for SGOI fabrication.

The coupling between the sSi thickness and the underlying layers is eliminated in the case of sSOI. The quality of the sSi for sSOI is related to sharpness of the sSi/SiGe interface of the donor wafer, first to maximize the selectivity to Si during removal of the remaining SiGe after layer transfer, and second because it determines the resulting surface roughness (typical 1.3Å rms for 1x1µm, 2Å rms for 10x10µm).

Raman Characterization

Macro and micro Raman measurements have proven to be essential to accurately characterize the Ge content and the degree of relaxation of SiGe, and on the other hand, the stress level in the sSi film. UV and visible Raman spectra are used to fully characterize the donor wafers as well as the finished sSOI and SGOI. The Raman technique is calibrated with XRD, SIMS and RBS measurements [15]. A very good correlation between calculated and measured values is achieved as shown in Fig. 4.

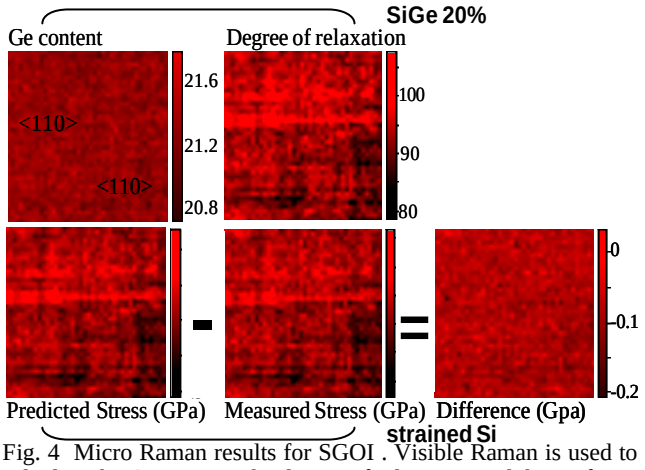

Fig. 4 Micro Raman results for SGOI . Visible Raman is used to calculate the Ge content, the degree of relaxation and the uniformity over a 40x40m area. UV Raman measures directly the stress in the sSi film. The agreement between the calculated and measured sSi stress is within 10%.

3. Conclusions

A review of the manufacturing issues of strained SOI has been given. In spite of the strong synergy with the already proven Smart Cut technology for SOI high volume production, the fabrication of SGOI and sSOI presents new challenges. The optimization of the donor material will have to continue to progress reducing defectivity and improving the level of strain and its homogeneity over the wafer. Furthermore, new metrology will have to introduced to monitor the reproducibility and level of strain.

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