Double Gate SOI MOSFET – Considerations for Improved Cut-off Frequency

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1. Introduction

In recent years much attention has been devoted to the study of dc characteristics of Double Gate (DG) MOSFETs owing to the inherent suppression of short channel effects, improved current drive (I_ds) and excellent scalability. Results from the dc analysis have shown that the transconductance (g_m) of a DG MOSFET is nearly 2 times as that of a Single Gate (SG) MOSFET [1]. We investigate for the first time, by detailed ac simulations, whether this challenge to produce thin and uniform monocrystalline silicon layer (< 10 nm); (ii) use HALO implants with problematic increase of global doping level for ultra-short channel devices, and reduction of effective mobility.

2. Device Simulation

In the DG and SG devices (Fig. 1) analyzed, the thickness of gate oxide, silicon film and buried oxide were 2 nm, 20 nm and 150 nm, respectively. The silicon film doping was 10^{15} cm^{-3} and channel length (L) for these devices was varied from 50 nm to 500 nm. The devices analyzed here have been simulated using a commercial numerical simulator, SILVACO [2] using Energy Balance model with default parameters. The gate electrode workfunction was taken to be 4.67 eV which corresponds to Molybdenum [3]. The physical models accounting for electric field dependent carrier mobility with velocity saturation, SRH recombination/generation with doping dependent lifetime, Auger recombination, bandgap narrowing, self and lattice heating and impact ionization were included. For the ac small signal characteristics, a small signal with frequency from 1 MHz to 200 GHz and amplitude of 30 mV was considered. The gate is used as the inport and drain as the outport with a common source configuration.

3. Results and Discussions

Table 1 shows the description of various DG and SG devices simulated in our work. Threshold voltage (V_th) was extracted as the gate voltage when the drain current reached the value of 1.127xW/L μA. Subthreshold slope (S) and DIBL (=\Delta V th/\Delta V ds) values calculated for various devices show clearly the advantages of DG MOSFETs due to excellent charge control. In order to improve the short channel effects (SCE) in SG devices, we need to (i) reduce the thickness of the silicon film, with the technological

3.1. DC analysis

Fig. 2 shows the extracted mobility (\mu) and electron concentration (n_e) at the surface and center of the silicon film for a DG MOSFET for L=100 nm and Vds=1 V. At lower gate bias (Vgs), the carriers spread out across the silicon film thus indicating the presence of volume inversion (VI) whereas at higher Vgs, the carriers at surface screen the carriers at the centre. As a result the rate of increase of n_e is much higher at the surface than at the centre. Despite the high \mu due to reduced vertical electric field at the centre, surface \mu dominates the conduction at high Vgs where the DG device behaves as a two channel device as n_e at the surface is nearly an order of magnitude higher than that at the centre of film.

Fig. 3 shows the dependence of g_m/I_ds on I_ds/(W/L) at Vds=1 V. Ideal values (~38 V^{-1}) of g_m/I_ds (for L ≥ 100 nm) are achieved by DG devices due to the improved charge control which leads to reduced body effect as compared to the SG devices. As L is reduced, the effect of gate control in the DG becomes clear whereas SG only achieve a g_m/I_ds of 29 V^{-1} (for L=100 nm) compared to the near ideal value for the DG device. At g_m/I_ds of 33 V^{-1}, an increase in I_ds/(W/L) by a factor of 6 is observed between DG and SG for devices with L ≥ 200nm, whereas at g_m/I_ds of 5 V^{-1}, an increase by factor of 2 is observed for devices with L ≤ 50nm. The increase in
current ratio ($I_{dsDG}/I_{dsSG}$) by a factor of 6 is due to the presence of VI effect in DG devices whereas at higher gate biases, DG MOSFET behaves as a dual-channel device and the improvement in the current ratio is only by a factor of 2. These results present here are consistent with the previously reported results for the DG devices [4].

Fig. 4 shows the ratio of $g_m$ values between the DG and SG devices with gate overdrives. At low $V_{go}$, the ratio $g_{mDG}/g_{mSG}$ is much higher than 2 and as the $V_{go}$ increases, this ratio tends towards 2. This increase in $g_{mDG}/g_{mSG}$ at lower $V_{go}$ is attributed to the VI where higher values of $g_m$ is due to high electron concentration and increased channel mobility as shown in Fig. 2. As $V_{go}$ increases, DG device works only as a two channel device and $g_{mDG}/g_{mSG}$ approaches 2. For $L=50$ nm, the $g_m$ ratio is very high due to the severe SCEs in the SG MOSFET whereas DG device can still operate with acceptable level of SCEs without any channel engineering process (HALOs, high doping, asymmetric channel profile).

3.2. AC analysis

Fig. 5 shows the conventional small signal equivalent circuit used for the extraction of intrinsic elements for DG and SG devices.

Fig. 6 shows the variation of cut-off frequency, $f_T$ ($g_{m}(2\pi C_{gs}C_{gd})$) for both the DG and SG devices. At higher $V_{go}$, $f_T$ values for DG and SG devices are nearly same at all channel lengths. This is because at higher $V_{go}$, $g_{mDG}/g_{mSG}$ and $C_{gsDG}/C_{gsSG}$ approach 2 and any improvement in $g_m$ value is compensated by an equal increase in the capacitance in DG device as compared to SG structure. However, at smaller channel lengths ($L=50$ nm) and at lower $V_{go}$, a significant improvement in $f_T$ values achieved in DG devices is observed as compared to SG MOSFETs. This increase in $f_T$ is due to the higher gain in the $g_m$ value at lower $V_{go}$ (Fig. 4) for DG devices as compared to the SG MOSFETs. Even though there is an increase in the $C_{gs}$ value of DG devices compared to SG devices (Fig. 6), the increase is compensated by a much higher increase of $g_m$ value, thus leading to a significant increase in $f_T$ values at low $V_{go}$.

4. Conclusions

We investigated for the first time the dynamic performance of DG and SG devices to examine their potential for RF applications. DG devices show a significant improvement in S-slope, DIBL, $g_{m}/I_{ds}$, $C_{gs}/C_{gd}$ values due to improved charge control. The current ratio ($I_{dsDG}/I_{dsSG}$) at low $V_{go}$ can be significantly higher than 2 depending on VI in DG devices. Although the $g_m$ of DG devices is nearly twice that of SG devices, at higher $V_{go}$, the increased values of $C_{gs}$ of DG MOSFET result in nearly the same values of $f_T$ as that of SG devices. However, at ultra short channel lengths ($L \leq 50$ nm) and lower gate overdrives ($V_{go} \leq 400$ mV), DG devices shows significantly higher values of $f_T$ as compared to SG devices, thus presenting DG MOSFET as a serious candidate for microwave applications.

3. References