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Double Gate SOI MOSFET – Considerations for Improved Cut-off Frequency

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1. Introduction

In recent years much attention has been devoted to the study of dc characteristics of Double Gate (DG) MOSFETs owing to the inherent suppression of short channel effects, improved current drive (I_{ds}) and excellent scalability. Results from the dc analysis have shown that the transconductance (g_m) of a DG MOSFET is nearly 2 times as that of a Single Gate (SG) MOSFET [1]. We investigate for the first time, by detailed ac simulations, whether this increase in g_m can be translated into a corresponding improvement in cut-off frequency (f_T) of DG devices operating in saturation. We also analyze in detail the key figures of merit – intrinsic gate capacitances and their ratios, g_m and f_T of DG and SG devices to assess their potential for microwave analog applications. Our results show that only at low gate overdrives ($V_{go}=V_{gs}-V_{th}$) and ultra short channel lengths ($L \leq 50$ nm), a significant improvement in f_T of a DG MOSFET can be achieved over SG devices. We analyze comprehensively the conditions under which higher f_T values can be obtained for DG MOSFETs over SG devices.

2. Device Simulation

In the DG and SG devices (Fig. 1) analyzed, the thickness of gate oxide, silicon film and buried oxide were 2 nm, 20 nm and 150 nm, respectively. The silicon film doping was 10^{15} cm^{-3} and channel length (L) for these devices was varied from 50 nm to 500 nm. The devices analyzed here have been simulated using a commercial numerical simulator, SILVACO [2] using Energy Balance model with default parameters. The gate electrode workfunction was taken to be 4.67 eV which corresponds to Molybdenum [3]. The physical models accounting for electric field dependent carrier mobility with velocity saturation, SRH recombination/generation with doping dependent lifetime, Auger recombination, bandgap narrowing, self and lattice heating and impact ionization were included. For the ac small signal characteristics, a small signal with frequency from 1 MHz to 200 GHz and amplitude of 30 mV was considered. The gate is used as the inport and drain as the outport with a common source configuration.

3. Results and Discussions

Table 1 shows the description of various DG and SG devices simulated in our work. Threshold voltage (V_{th}) was extracted as the gate voltage when the drain current reached the value of $1.127\times W/L$ μA. Subthreshold slope (S) and DIBL ($=\Delta V_{th}/\Delta V_{ds}$) values calculated for various devices show clearly the advantages of DG MOSFETs due to excellent charge control. In order to improve the short channel effects (SCE) in SG devices, we need to (i) reduce the thickness of the silicon film, with the technological challenge to produce thin and uniform monocrystalline silicon layer (< 10 nm); (ii) use HALO implants with problematic increase of global doping level for ultra-short channel devices, and reduction of effective mobility.

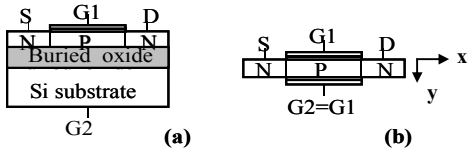

Fig. 1: Schematic diagram of (a) SG SOI MOSFET and (b) DG MOSFET.

Table 1: Description of SG and DG simulated in the present work.

L (nm)	t_{si} (nm)	V_{ds} (V)	V_{th} (V)		S (mV/dec)		DIBL (mV/V)	
			SG	DG	SG	DG	SG	DG
500	20	0.05	0.37	0.37	62.7	59.5	42	11
		1.00	0.33	0.36	61.1	59.4		
200	20	0.05	0.30	0.36	65.7	59.7	21	11
		1.00	0.28	0.35	65.7	59.9		
100	20	0.05	0.33	0.36	79.7	61.1	95	21
		1.00	0.24	0.34	82.2	61.2		
75	20	0.05	0.33	0.35	97.6	63.7	211	32
		1.00	0.13	0.32	128.6	63.9		
50	20	0.05	0.24	0.33	170.6	74.3	515	84
		1.00	-0.25	0.25	588.9	77.2		
50	15	0.05	0.33	0.35	115.1	67.5	263	53
		1.00	0.08	0.30	153.5	68.6		
50	10	0.05	0.34	0.37	86.9	63.1	168	42
		1.00	0.18	0.33	92.1	63.2		

3.1. DC analysis

Fig. 2 shows the extracted mobility (μ) and electron concentration (n_s) at the surface and center of the silicon film for a DG MOSFET for L=100 nm and V_{ds}=1 V. At lower gate bias (V_{gs}), the carriers spread out across the silicon film thus indicating the presence of volume inversion (VI) whereas at higher V_{gs}, the carriers at surface screen the carriers at the centre. As a result the rate of increase of n_s is much higher at the surface than at the centre. Despite the high μ due to reduced vertical electric field at the centre, surface μ dominates the conduction at high V_{gs} where the DG device behaves as a two channel device as n_s at the surface is nearly an order of magnitude higher than that at the centre of film.

Fig. 3 shows the dependence of g_m/I_{ds} on $I_{ds}/(W/L)$ at V_{ds}=1 V. Ideal values (~38 V^{-1}) of g_m/I_{ds} (for $L \geq 100$ nm) are achieved by DG devices due to the improved charge control which leads to reduced body effect as compared to the SG devices. As L is reduced, the effect of gate control in the DG becomes clear whereas SG only achieve a g_m/I_{ds} of 29 V^{-1} (for L=100 nm) compared to the near ideal value for the DG device. At g_m/I_{ds} of 33 V^{-1}, an increase in $I_{ds}/(W/L)$ by a factor of 6 is observed between DG and SG for devices with $L \geq 200$nm, whereas at g_m/I_{ds} of 5 V^{-1}, an increase by factor of 2 is observed for devices with $L \leq 50$nm. The increase in

current ratio (I_{dsDG}/I_{dsSG}) by a factor of 6 is due to the presence of VI effect in DG devices whereas at higher gate biases, DG MOSFET behaves as a dual-channel device and the improvement in the current ratio is only by a factor of 2. These results present here are consistent with the previously reported results for the DG devices [4].

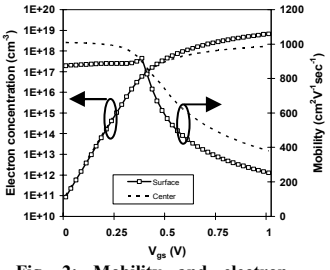

Fig. 2: Mobility and electron concentration extracted at surface and centre of silicon film at x=L/2 for DG MOSFET.

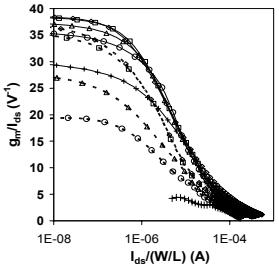

Fig. 3: g_m/I_{ds}-I_{ds}/(W/L) for DG and SG MOSFET. — DG - - - SG, + 50 nm, O 75 nm, Δ 100 nm, □ 200 nm, ◊ 500 nm

Fig. 4 shows the ratio of g_m values between the DG and SG devices with gate overdrives. At low V_{go}, the ratio g_{mDG}/g_{mSG} is much higher than 2 and as the V_{go} increases, this ratio tends towards 2. This increase in g_{mDG}/g_{mSG} at lower V_{go} is attributed to the VI where higher values of g_m is due to high electron concentration and increased channel mobility as shown in Fig 2. As V_{go} increases, DG device works only as a two channel device and g_{mDG}/g_{mSG} approaches 2. For L=50 nm, the g_m ratio is very high due to the severe SCEs in the SG MOSFET whereas DG device can still operate with acceptable level of SCEs without any channel engineering process (HALOs, high doping, asymmetric channel profile).

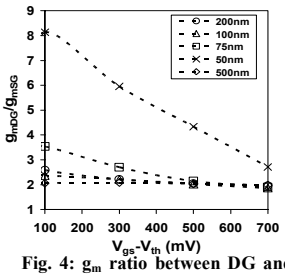

Fig. 4: g_m ratio between DG and SG devices extracted at V_{ds} = 1 V.

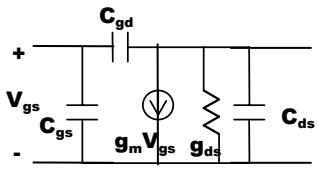

Fig. 5: Conventional small signal equivalent circuit used for the extraction of intrinsic elements for DG and SG devices.

3.2. AC analysis

Fig. 5 shows the conventional small signal equivalent circuit assumed to be valid for both DG and SG devices. Fig. 6 shows the ratio of the gate-source capacitance (C_{gs}) of DG and SG devices. At lower V_{go} values, an increase in C_{gsDG}/C_{gsSG} ratio is observed and its value approaches 2 at higher V_{go}. The increase in C_{gsDG}/C_{gsSG} ratio at lower V_{go} is due to VI in the DG devices. However, for the device with L=50 nm, a drastic reduction in C_{gsDG}/C_{gsSG} ratio at lower V_{go} is observed due to severe SCEs in SG MOSFETs. Fig. 7 shows the variation of C_{gs}/C_{gd} ratio for both DG and SG devices. C_{gs}/C_{gd} ratio decreases with scaling down of L for both DG and SG devices [5]. A decrease of this ratio means a loss of channel charge control by the gate and an increase of parasitic feedback gate-drain capacitance (C_{gd}). DG devices achieve a higher value of C_{gs}/C_{gd} ratio as compared to SG devices at all channel lengths and gate overdrives.

Fig. 8 shows the variation of cut-off frequency, f_T ($=g_m/(2\pi(C_{gs}+C_{gd}))$) for both the DG and SG devices. At higher V_{go}, f_T values for DG and SG devices are nearly same at all channel lengths. This is because at higher V_{go}, g_{mDG}/g_{mSG} and C_{gsDG}/C_{gsSG} approach 2 and any improvement in g_m value is compensated by an equal increase in the capacitance in DG device as compared to SG structure. However, at smaller channel lengths (L=50 nm) and at lower V_{go}, a significant improvement in f_T values achieved in DG devices is observed as compared to SG MOSFETs. This increase in f_T is due to the higher gain in the g_m value at lower V_{go} (Fig. 4) for DG devices as compared to the SG MOSFETs. Even though there is an increase in the C_{gs} value of DG devices compared to SG devices (Fig. 6), the increase is compensated by a much higher increase of g_m value, thus leading to a significant increase in f_T values at low V_{go}.

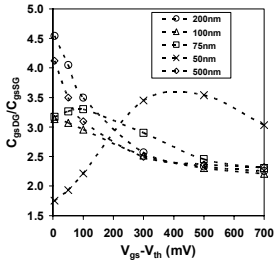

Fig. 6: C_{gsDG}/C_{gsSG} ratio for DG and SG devices at V_{ds} = 1 V.

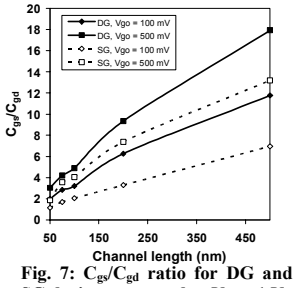

Fig. 7: C_{gs}/C_{gd} ratio for DG and SG devices extracted at V_{ds} = 1 V.

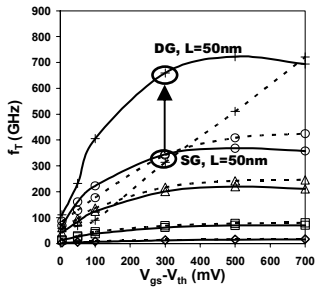

Fig. 8: Cut-off frequency for DG and SG MOSFETs at V_{ds} = 1 V. — DG - - - SG; + 50 nm, O 75 nm, Δ 100 nm, □ 200 nm, ◊ 500 nm.

4. Conclusions

We investigated for the first time the dynamic performance of DG and SG devices to examine their potential for RF applications. DG devices show a significant improvement in S-slope, DIBL, g_m/I_{ds} and C_{gs}/C_{gd} values due to improved charge control. The current ratio (I_{dsDG}/I_{dsSG}) at low V_{go} can be significantly higher than 2 depending on VI in DG devices. Although the g_m of DG devices is nearly twice that of SG devices, at higher V_{go}, the increased values of C_{gs} of DG MOSFET result in nearly the same values of f_T as that of SG devices. However, at ultra short channel lengths (L ≤ 50 nm) and lower gate overdrives (V_{go} ≤ 400 mV), DG devices shows significantly higher values of f_T as compared to SG devices, thus presenting DG MOSFET as a serious candidate for microwave applications.

3. References

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