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30-day-long Data Retention in Ferroelectric-gate FETs with HfO_2 Buffer Layers

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1. Introduction

One transistor-type (1T-type) ferroelectric random access memories (FeRAM) is one of the most promising ultimate non-volatile memories [1]. However, they have not been put into practical use until now, because of poor interface properties between the ferroelectric film and Si substrate. In this study, metal-ferroelectric-insulator-semiconductor (MFIS) diodes and FETs (field-effect-transistors) are fabricated using HfO_2 as insulating buffer layers. Their ferroelectric films are $SrBi_2Ta_2O_9$(SBT) and $(Bi,La)_4Ti_3O_{12}$(BLT). As a result, 30-day-long data retention was demonstrated for the first time.

2. Experiment

Figure 1 shows the illustration of a fabricated p-channel MFIS FET. HfO_2 thin films were deposited by a ultra-high-vacuum (UHV) electron-beam (EB) evaporation method, and then annealed in a rapid-thermal-annealing (RTA) furnace at 800 °C for 1min in O_2 flow. The physical thickness of HfO_2 thin films is presumed to be about 10 nm. The ferroelectric films such as SBT and BLT were deposited by a sol-gel method. Finally, the ferroelectric films were crystallized at 750 °C for 30min in O_2 flow by RTA. The total thickness of both SBT and BLT were about 400nm. Then, Pt top electrodes were formed by etching a uniform film using a reactive ion etching (RIE) apparatus with Ar and Cl_2 gases. The source and drain contact holes were formed by using wet and dry etching. Finally, Al electrodes were patterned by lift-off process. The samples were sintered at 450°C for 5min in N_2 flow.

3. Results and discussion

Figure 2 (a) shows the capacitance-voltage (C-V) characteristic of a MIS diode measured at 1MHz. As can be seen from the figure, no hysteresis loop was observed after RTA at 800 °C for 1min in O_2 flow. Therefore, an excellent interlayer property between the HfO_2 buffer layer and Si substrate was expected. Equivalent-oxide-thickness (EOT) calculated from the accumulation capacitance of HfO_2 is 3.6nm. Figure 2 (b) shows the leakage current density characteristic for the same sample as that in Fig.2(a). The current density at 2V is about 5×10^{-7} A/cm^2.

Figure 3 (a) shows 1MHz C-V characteristic of the BLT/HfO_2 diode. The curve has a hysteresis loop with a counterclockwise direction, and the memory window width is about 1V. Figure 3 (b) shows the leakage current density characteristic. The current densities at ±5V are on the order of 10^{-9} A/cm^2, which indicates that the leakage current characteristic of the MFIS diode is excellent. The capacitance retention characteristic of the BLT/HfO_2 sample is shown in Fig.4. As can be seen from this figure, the capacitance values are clearly distinguishable for over 5 days.

Figure 5 shows drain current-gate voltage (I_D-V_{GS}) characteristics of the MFIS FETs with SBT/HfO_2 and BLT/HfO_2 gate structures. I_D-V_{GS} characteristics show clockwise hysteresis due to polarization reversal in the ferroelectric films. The memory window width of the hysteresis loop is about 1.0V in the SBT/HfO_2 sample and it is about 0.5V in the BLT/HfO_2 sample. It was also found in the BLT/HfO_2 sample that the drain current on/off ratio was as large as 200 even if the "write" pulse width was decreased to 20ns.

Figure 6 shows retention characteristics of the MFIS FETs with the SBT/HfO_2 and BLT/HfO_2 structures. In these measurements, the "write" pulses of ±10V in amplitude and 1μs in width were initially applied to the gate, and variation of drain currents was measured, keeping the gate voltages at 0.6V and 0.3V in the SBT/HfO_2 and BLT/HfO_2 samples, respectively. In the BLT/HfO_2 sample, the drain current on/off ratio was larger than 10^2 at 10 days after "write" operation. More interestingly, it was larger than 10^3 in the SBT/HfO_2 sample even after 30 days had elapsed. This retention time is about three times longer than the so-far reported longest one [2].

4. Conclusions

We investigated the electrical properties of MIS and MFIS diodes, as well as p-channel MFIS FETs. The fabricated SBT/HfO_2 sample exhibited the drain current on/off ratio larger than 10^3 even after 30 days had elapsed. It is concluded from these results that the ferroelectric/HfO_2 structure is one of the most promising candidates for realizing FET-type ferroelectric random access memories with long data retention.

References

[1] L. Moll and Y. Tarui, *IEEE Trans. Electron Devices, ED-10, 333 (1963).*
[2] S. Sakai et al. , *IEEE Electron Device Lett. (in press)*

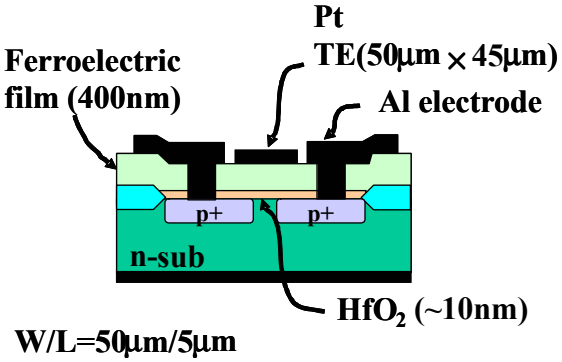

Fig.1 Illustration of a fabricated p-channel MFIS FET.

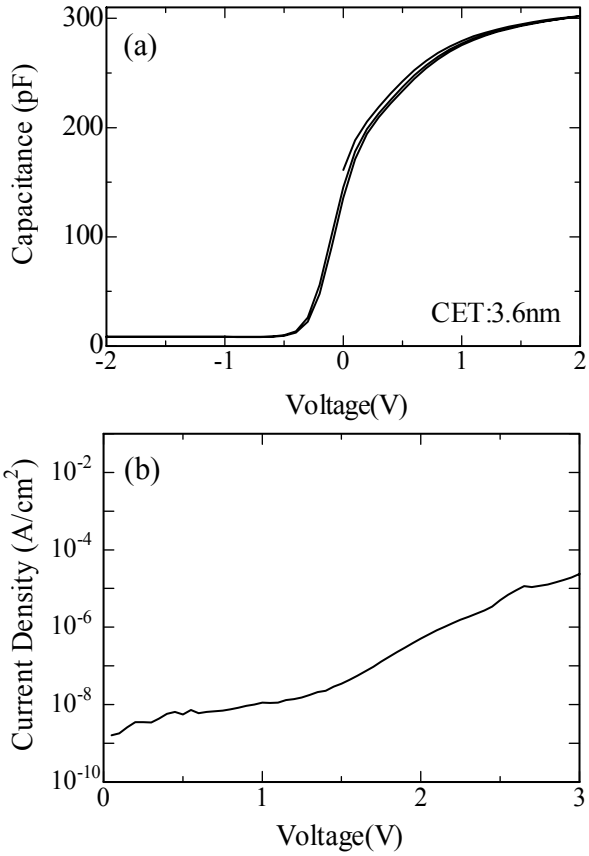

Fig.2 (a) C-V and (b) I-V characteristics of MIS diode.

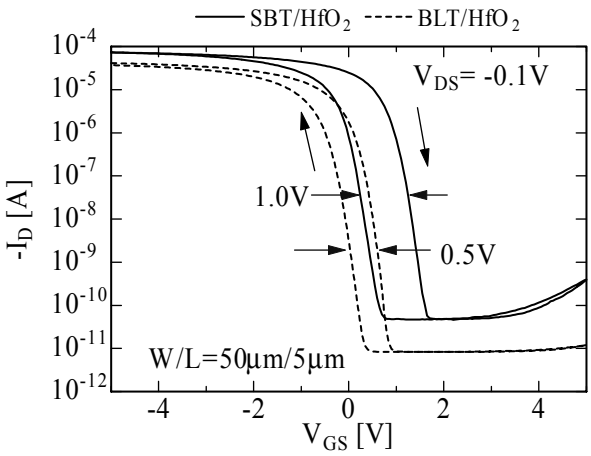

Fig.5 I_D-V_{GS} characteristics of MFIS FETs.

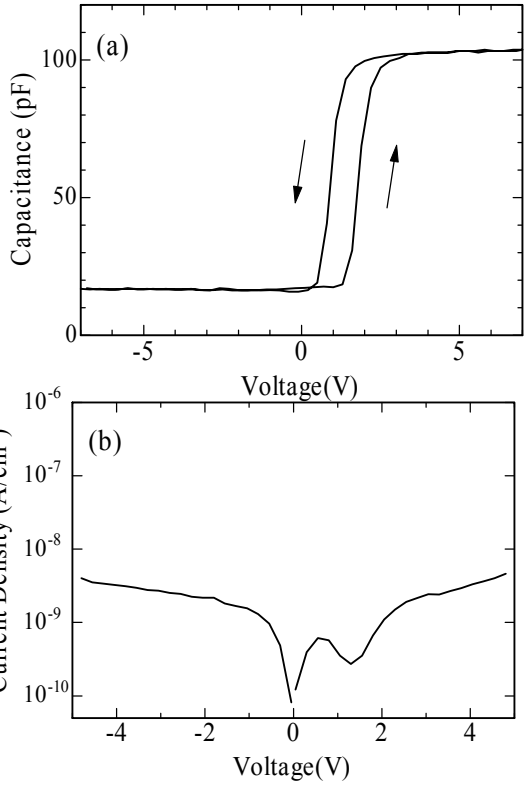

Fig.3 (a) C-V and (b) I-V characterisitics of MFIS diode.

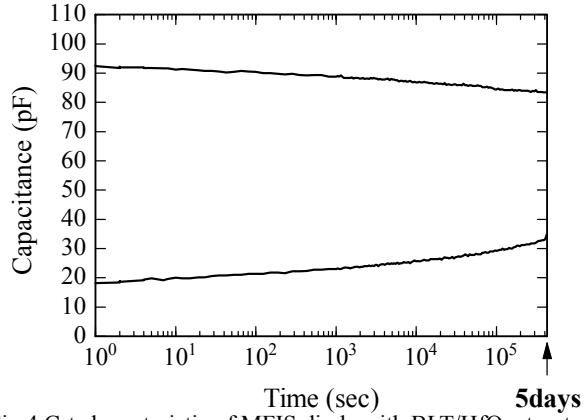

Fig.4 C-t characteristic of MFIS diode with BLT/HfO_2 structure.

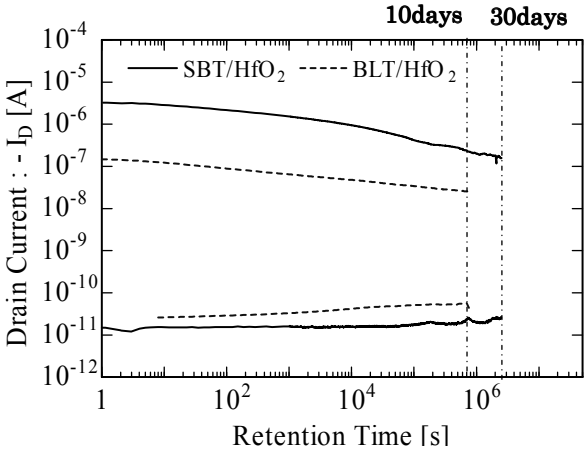

Fig.6 Retention characteristics of MFIS FETs.