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Fabrication and Characterization of 1k-bit 1T2C-Type Ferroelectric Memory Cell Array

Hyun-Soo Kim[1], Shuu'ichirou Yamamoto[1], Toru Ishikawa[2] and Hiroshi Ishiwara[1]

[1] Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology,
4259 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan
Phone: +81-45-924-5122 E-mail: hskim@neuro.pi.titech.ac.jp
[2] R&D Association for Future Electron Devices, 2-9-14 Toranomon, Minato-ku, Tokyo 105-0001, Japan

1. Introduction

A 1T2C-type ferroelectric memory cell shown in Fig. 1 has such a structure that two ferroelectric capacitors with the same area are connected to the gate of a MOSFET, and it has been reported by the previous studies that this type of cell has such advantages as non-destructive data readout with a high current on/off ratio and excellent data retention time [1, 2]. In this study, we designed and fabricated a 1k-bit 1T2C-type ferroelectric memory cell array and characterized the basic operations of a selected memory cell in the array structure.

2. Fabrication of 1k-bit 1T2C-type ferroelectric memory cell array

Using a 0.35μm process technology for CMOS parts and a 3μm design rule for ferroelectric capacitors and interconnections, a 1T2C-type memory cell array was designed and fabricated. The two different processes were combined at the first CMOS metallization stage as shown in Fig. 2. Fabrication processes are as follows; a TiN layer of 100nm in thickness was deposited on a 3" wafer and patterned for formation of connection pads. SiO_2/Al_2O_3 insulating layer of 0.7μm/10nm in thickness was deposited on it and annealed at 700°C for 30min in O_2 atmosphere. Since the sputtered Al_2O_3 layer acts as an oxygen diffusion barrier, oxidation of TiN is prevented. On this structure, a $Pt(100nm)/Sr_{0.8}Bi_{2.2}Ta_2O_9(120nm)/Pt(200nm)/Ti(20nm)$ multi-layer was formed by RF sputtering and sol-gel methods. The gel thin films were spin-coated at 2500rpm for 30s, dried at 180°C for 5min, and pre-fired at 700°C for 1min in O_2 atmosphere. These processes were repeated four times to obtain a desired film thickness. The second SiO_2/Al_2O_3 insulating layers were deposited on the Pt/SBT/Pt/Ti capacitors patterned in a staircase by Ar/Cl_2 reactive ion etching, and annealed at 700°C for 30min in O_2 atmosphere. In this case, Al_2O_3 plays a role of a barrier layer for hydrogen during plasma enhanced chemical vapor deposition using TEOS. Finally, contact holed and Pt(200nm)/Ti(20nm) interconnections were formed by reactive ion etching and RF sputtering.

Figure 3 shows a microphotograph of the 1T2C-type ferroelectric memory array. Occupied area of the unit memory cell is $0.05mm^2$. Top electrode of ferroelectric capacitors in the memory cell is 9μm×9μm in size. Gate length and width of a transistor in the memory cell array are 18μm and 90μm so that the ratio S_{OX}/S_F between the ferroelectric capacitor area S_F and the transistor gate area S_{OX} becomes 20.

3. Operation characteristics

The 1k-bit 1T2C-type ferroelectric memory array has 32 cells in row and column lines, respectively. Figure 4 shows the drain current versus gate voltage characteristics of MFMIS (metal-ferroelectric-metal-insulator-semiconductor) structure which is composed of one ferroelectric capacitor and a MOSFET. It can be seen that the distributed cells in the memory array have almost the same electrical properties, as well as the ferroelectric capacitors and MOSFET were successfully fabricated.

Figure 5 shows the output current characteristics of the selected memory cell for binary data "0" and "1" when the various readout voltages are applied to the terminal B, keeping A open. In this measurement, the writing pulses of ±3V in amplitude and 200ms in width were applied. This data writing method can be used to estimate the maximum current on/off ratio of a single memory cell since the disturbance voltages are not applied to the ferroelectric capacitors. It was found that the maximum current on/off ratio of the fabricated memory cell is as large as 7200. However, we can not use this method for writing data in a selected memory cell in an array from the periphery circuit, but we have to use the V/3 rule [3] or other modified methods by which the data disturbance effect can not be avoided.

Figure 6 shows the output current characteristics of the selected memory when data are written using the V/3 rule. Pulses of 3V and 1V with 10ns width were first applied to the terminals of ferroelectric capacitors, keeping the Si substrate grounded, and -1V and -3V were applied in the next timing. It can be seen from the results that the drain current on/off ratio was about two orders of magnitude even under the disturbance condition.

4. Conclusions

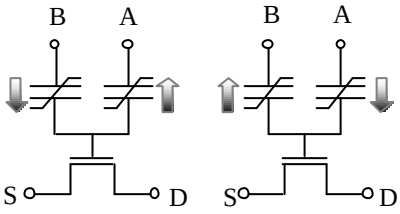
We fabricated a 1k-bit 1T2C-type ferroelectric memory cell array and investigated the electrical properties of a selected memory cell in the array structure. The current on/off ratio of 230 was obtained in writing and reading operations to a selected cell in a memory array. We conclude from these results that a 1T2C-type memory array is promising as a future ferroelectric memory.

References

[1] H.Ishiwara, Integrated Ferroelectrics, 34 (2000) 11

[2] S.M. Yoon and H. Ishiwara, IEEE Trans. Electron Devices, 48 (2001) 2002

[3] H.Ishiwara and S.Yamamoto, Proc.23rd Int. Conf. Microelectronics, pp-517-520 (2002)



(a) Datum "0" (b) Datum "1"

Fig. 1. Equivalent circuits of 1T2C-type ferroelectric memory

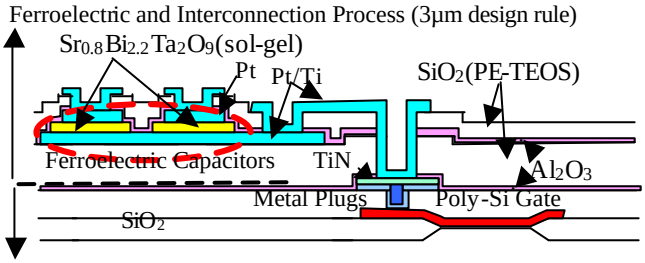


Fig. 2. Cross-sectional view of a 1T2C-type ferroelectric memory cell.

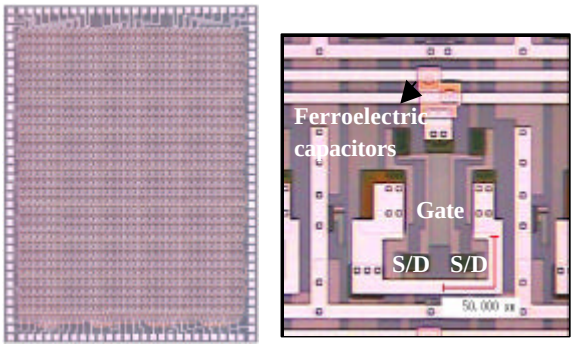


Fig. 3. Microphotographs of the fabricated 1T2C-type ferroelectric memory cell array.

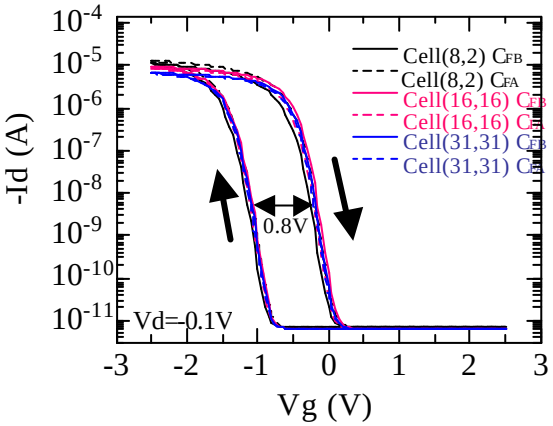
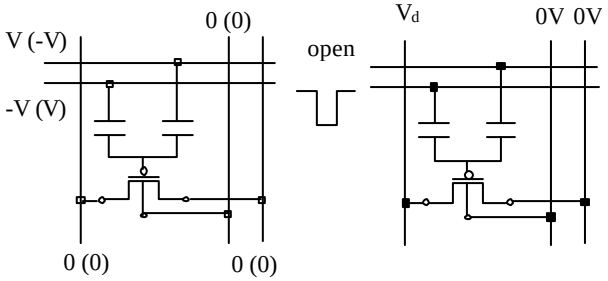
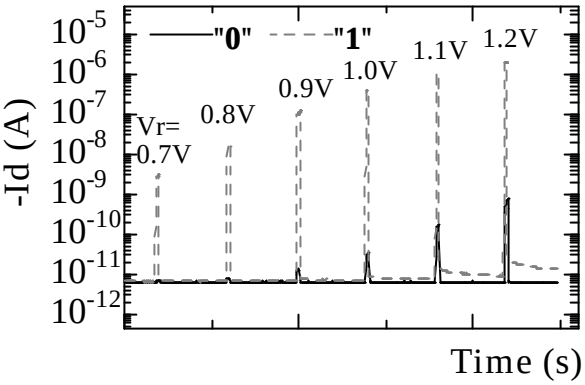


Fig. 4. Id-Vg characteristics of MFMIS structure

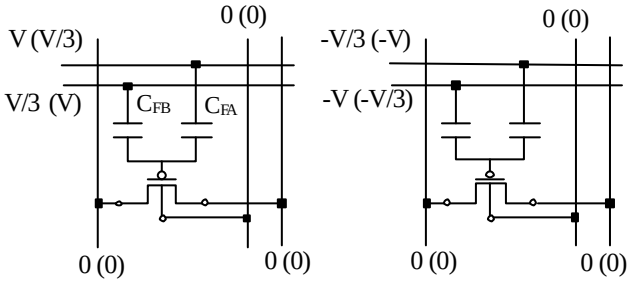


(a) Writing operation (b) Readout operation

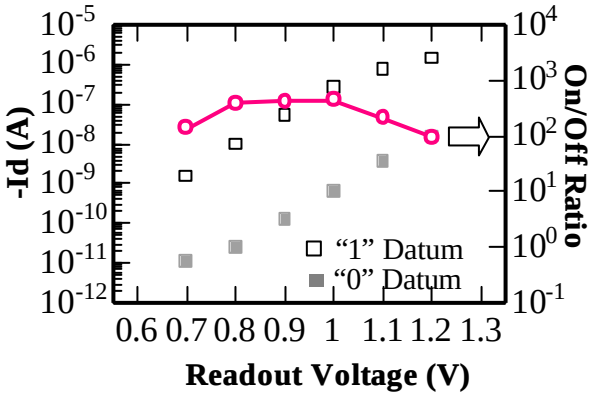


(c) Output drain currents

Fig. 5. Writing and readout operation of the fabricated 1T2C-type cell



(a) V/3-rule data writing method



(b) Readout drain currents and current on/off ratio

Fig. 6. Writing and readout operation with V/3-rule data writing method in memory array structure