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Robust 3-Metallization BEOL Process for 0.18 μm Embedded FRAM

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1. Introduction

Ferroelectric random access memories (FRAM) are presently the object of intensive studies due to their ideal properties such as non-volatility, fast write/read time, and low power consumption. In one of our recent papers, we reported on a stand-alone FRAM device with 0.25 μm design rule, $15F^2$ cell size, and 1 transistor / 1 capacitor (1T1C) structure and demonstrated its high reliability[1]. However, a problem still to be solved is large cell size which limits the storage density of the device. Thus in order to compete as stand-alone devices with market-leading memory devices such as dynamic random access memories (DRAM) and Flash memories, future development of a 3-dimentional capacitor structure is indispensable. Nevertheless, even at the present stage, there exist promising application fields for FRAM devices. One example is FRAM embedded smartcard for mobile electronics where speed in addition to non-volatility can play a key role in future high-speed applications[2,3]. Present smartcards typically use electrically erasable programmable read only memories (EEPROM) as storage device. Low endurance properties and the update time delay are critical drawbacks of EEPROMs, which can be overcome by using FRAMs instead for future high-speed applications. However, integrating FRAM memories into conventional smartcard fabrication can cause degradation of the ferroelectric cells because of incompatible process steps. In this study, we address these problems and demonstrate key process parameters and a novel scheme for fabricating an FRAM embedded smartcard device with 0.18 μm design rule.

2. Experimental Procedure and Device Features

In the following, we describe the basic process steps used for fabricating the ferroelectric capacitors. The capacitor stacks are built on a conventional W-plugged CMOS substrate. A TiAlN/Ir layer is deposited on tungsten buried contact (BC). This is followed by metal-organic chemical vapor deposition (MOCVD) of $Pb(Zr_xTi_{1-x})O_3$ (PZT) and subsequent IrO_2/Ir top electrode deposition. A one-step mask etch scheme is used for patterning, resulting in a capacitor size of 0.59 μm^2. Finally, an encapsulating barrier layer (EBL) is grown to protect the capacitor from hydrogen damage during the following integration process. The backend integration process consists of ILD and IMD oxide deposition, triple aluminum metallization and W-plugs (MC, Via1, Via2). EBLs for capacitor protection are applied several times during the integration process. A plain-view image and a schematic vertical structure of the 0.18 μm design-ruled FRAM embedded smartcard device are displayed in Fig. 1 (a) and (b). The device contains a 128 KB (64 KB + 64 KB) FRAM for data storage, a 384 KB Mask ROM as code memory, and an 8 KB FRAM as buffer memory. EEPROM and SRAM which served as data memory and buffer memory respectively, in the original device, are replaced by FRAMs.

3. Key Technologies for Smartcard Architecture

Integration of FRAMs into an embedded smartcard requires various modifications to architecture and backend integration processes. Smartcard logic devices require tighter design rules than stand-alone FRAMs as well as relatively thick inter-metal oxide layers to prevent interference between metal lines. This results in higher aspect ratios for both metal contacts and metal lines. On the other hand, for ferroelectric capacitors stricter conditions than for the EEPROM embedded smartcard have to be imposed on backend integration processes, since ferroelectric capacitor easily degrades when improper processes are used.

Optimization of Barrier Metal (BM) and W Deposition Scheme

Al, which was originally used as a metal interconnection material in the stand-alone FRAM device, cannot be used in the FRAM embedded smartcard. Increased aspect ratios result in high contact resistances (R_c) and even contact fails. Although conventional CVD tungsten is generally the standard solution for interconnection plugs in logic devices, high hydrogen contents and high temperatures during deposition complicate the use for FRAMs. This is shown in Fig. 2, where the sensing window is shown for Al and W-plugged stand-alone FRAM devices, respectively. The small sensing window for the W plug case indicates that degradation of the capacitor due to hydrogen damage indeed occurs for conventional W-plugging. Optimizing W plug scheme by reducing hydrogen contents and/or lowering temperature during deposition results in a significantly reduced capacitor degradation, as shown in Fig. 3. The best results are achieved by a combination of the two factors.

The use of W-plugs requires the application of a barrier metal (BM) layer and an adapted etch scheme. As the standard high temperature BM process causes capacitor degradation, we utilized a deposition scheme with lowered temperatures. Additionally, we replaced the via etch stop to Al (VESA) etch scheme with via etch stop to TiN (VEST) scheme to achieve a stable and uniform distribution of R_c values. Results are summarized in Fig. 4 (a) and (b). It can be seen that degradation of the capacitor polarization is completely prevented and a uniform distribution of R_c is achieved.

IMD and EBL Process

The IMD deposition method used for EEPROM embedded smart cards is another critical integration process for ferroelectric capacitors. Hydrogen damage as well as stress exerted on the PZT films is possible causes of capacitor degradation. The conventional high density plasma (HDP) oxide, which is used because of its good step coverage properties, causes severe degradation of $2P_r$ values as can be seen in Fig. 5. As shown in the graph, a protective oxide buffer layer between HDP and capacitor reduces degradation to a certain extent. However, only a novel scheme utilizing an optimized oxide deposition procedure combined with a buffer layer shows satisfactory results. In spite of optimized backend processes, additional measures for protecting the ferroelectric PZT film are still necessary. As previously reported, multiple encapsulating barrier layers (EBL) for PZT protection were utilized. This remains valid also for the optimized backend scheme. In Fig. 6 (a) and (b), the effects of applying EBLs in combination with the altered backend processes are demonstrated. It is obvious that only a combination of all factors leads to a satisfactory result.

Ferroelectric Properties and Sensing Window

In order to investigate the effectiveness of the capacitor protecting scheme mentioned above, properties of the ferroelectric capacitors were measured at different levels of integration. In Fig. 6(b), $2P_r$ values of the capacitors are shown after the deposition of the capacitor stack, at the ATE level and after metal-3 deposition, respectively. It is seen that after backend integration $2P_r$ values still amount to 85% of the original values, which shows that an

effective protection of the capacitors is achieved. Improved capacitor properties result in a significantly increased sensing margin compared to the non-optimized integration scheme. As shown in Fig. 7, the optimized back end process leads to a large sensing margin of 380 mV between data "1" and "0", which is not far from the value of 420 mV for the previous stand-alone FRAM integration.

4. Conclusions

We discussed degradation of ferroelectric capacitor properties due to hydrogen and high temperature damage during backend processes in the viewpoint of integration into smartcard architecture. An optimized backend scheme was suggested, which consists of the application of low hydrogen and low temperature W-plug and BM deposition, an accordingly adapted via etch scheme, an optimized IMD oxide deposition, and the application of multiple EBLs. We demonstrated that capacitor degradation could almost completely be prevented through the combined application of the various optimized processes

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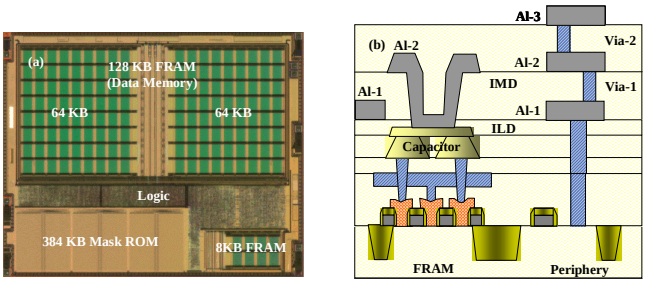

Fig. 1 (a) Layout image and (b) schematic illustration of FRAM embedded smartcard.

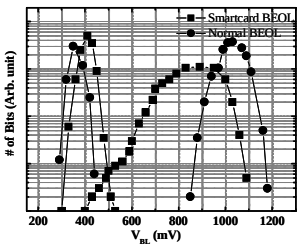

Fig. 2 Measured charge distributions after smartcard BEOL scheme and stand-alone BEOL scheme.

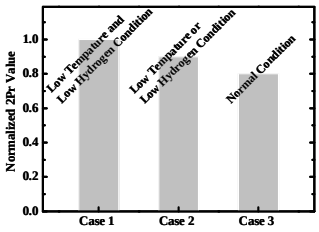

Fig. 3 Normalized $2P_r$ variation with W deposition scheme.

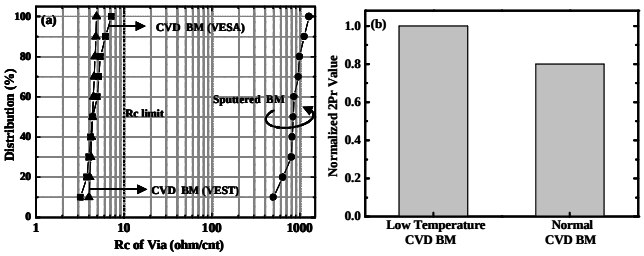

Fig. 4 (a) Distribution of R_c and (b) polarization variation with BM deposition method.

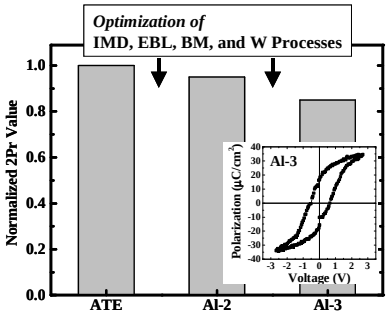

Fig. 5 Comparison of $2P_r$ at ATE, Al-2, and Al-3 integration step when all optimized conditions are employed. (P-V graph after Al-3 step is drawn, also.)

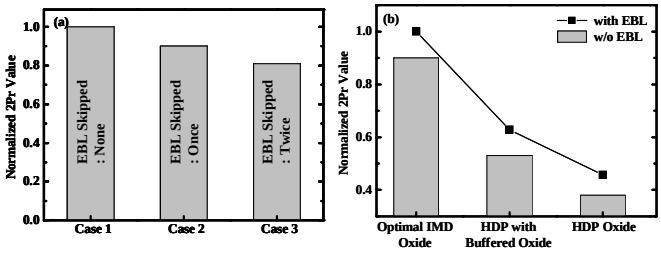

Fig. 6 Polarization trend as a function of (a) EBL and (b) IMD with or w/o EBL scheme.

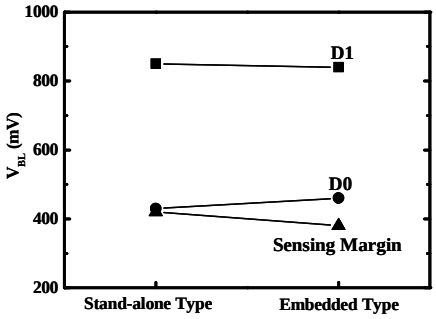

Fig. 7 Sensing margin of FRAM cell between stand-alone type and smartcard type.