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Recent Development in Phase Change Memory

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1. Introduction

Non-Volatile Memories (NVM) are playing a very important role in the semiconductor market, thanks in particular to Flash, used mainly in cellular phones and other types of electronic portable equipments (mobile PC, mp3 player, digital camera and so on). Also in the coming years portable systems will ask even more NVM either with high density and very high writing throughput for data storage application, or with fast random access for code execution in place, increasing the interest around a global NVM.

Although the Flash memory technology has been able to follow the evolution of the semiconductor roadmap, since its introduction in late'80s, and the further scaling down is forecasted to continue in the next coming years, there are some physical limitations to be faced and the downscaling beyond the 45nm technology node is still considered critical. Hence other technologies, alternative to floating gate devices, have been proposed and are under investigation. They exploit different physical mechanisms to store the information, like magnetism, ferroelectricity, solid electrolysis, phase change.

Among the different NVM, based on these mechanisms alternative to the floating-gate concept, Phase-Change Memories (PCM), also called Ovonic Unified Memory (OUM), are one of the most promising candidates to become mainstream NVM, having the potentiality to improve the performance compared to Flash - random access time, read throughput, direct write, bit granularity, endurance - as well as to be scalable beyond Flash technology.

2. The Concept

Some alloys based on the VI group elements (usually referred as chalcogenides) have the interesting characteristic to be stable at room temperature both in the amorphous and in the crystalline phase. In particular, the most promising are the GeSbTe alloys which follow a pseudobinary composition (between GeTe and Sb_2Te_3), hereafter referred as GST.

The PCM cell is essentially a resistor of a thin-film chalcogenide material with a low-field resistance that changes by orders of magnitudes, depending on the phase state of the GST in the active region. The switch between the two states occurs by means of local temperature increase. Above the critical temperature, the crystal nucleation and growth occur and the material becomes crystalline (Set operation). To bring the chalcogenide alloy back to the amorphous state (Reset operation), the temperature must be increased above the melting point of hundreds of ^{o}C and then very quickly quenched down in order to preserve the disorder and not let the material to crystallize. From an electrical point of view, it is possible to use the Joule effect to reach locally both critical temperatures using the current flow through the material by setting proper voltage pulses. The cell read out is performed at low bias. Programming thus requires a relatively large current, in order to heat-up the GST and lead to a thermally induced local phase change. Phase-transitions can be thus easily achieved by applying voltage pulses with different amplitudes and with durations in the range of tens of nanoseconds.

3. The Development

Although the phase change concept is well known since years and the first studies dates back to the '70s [1-3], its application for NVM has known renewed efforts after the year 2000. Phase change materials are nowadays extensively used in optical rewritable media (CD and DVD RW): the change of reflectivity between the amorphous and crystalline state store the information, and a semiconductor laser beam is used to thermally promote the transition between the two states. Since the two phases present also a different resistivity, the basic idea of solid state PCM is to use the low (crystalline) and high (amorphous) resistivity as logic 1 and 0, respectively. The information is therefore stored in the structural status of the material itself and the switching between the two (stable) states is induced by a proper electrical pulse

In 1999 the idea to have a semiconductor NVM cell based on the phase change of a chalcogenide material has been presented again [4-5]. Since then the effort to bring the PCM basic concept to a mature technology level has constantly increased and many groups have started to study, to develop and to integrate in Multi Megabit array the memory cell. As a demonstration of the interest and of the activities on PCM, in 2003 6 papers, related to the phase change memory technology, have been presented at the International Electron Devices Meeting [6-11].

Recently the PCM technology has reached the phase of large array demonstrator (from 8Mb to 64Mb) showing fast growing capabilities to reach the maturity for manufacturability [12-13].

4. The Cell Architecture

Considering the electronic and transport properties of the GST alloy, either in the crystalline or in the amorphous

state, in order to form a functional compact cell array, a PCM cell must be formed by the variable resistor (heater and GST – called data-storage) with in series a selector device (transistor). Hence, the basic PCM cell is has a 1T/1R structure. The type of transistor and of data-storage varies respectively as a function of the application and of the process architecture strategy.

For high-density memory, a more compact cell layout is achieved via the vertical integration of a pnp bipolar transistor [14-15], while for embedded memory the transistor is a n-channel MOS, where a larger cell size is balanced by a minimum process cost overhead with respect to the reference CMOS [14]. Only recently also a MOS-selected cell has been proposed for high density PCM, obtaining a compact cell layout thanks to a very narrow, but also a very short gate dimension [16]. A 3.5nm gate oxide transistor should provide the necessary reset current at 3V of supply voltage. In this approach, the process simplicity is balanced with a heavily stressed CMOS and the data-storage long endurance concern translated into MOSFET reliability.

The integration of the data-storage occurs between the front-end and the back-end of the CMOS process. The "simple" variable resistor, i.e. the heater and GST system, may be obtained in different way and the choice is a function of the understanding of process complexity, current performances, thermal properties and scaling perspective [7]. A possible approach is to use a sub-litho contact heater with a planar GST [17] or a modified version with a recession in the contact and GST confinement, which should improve the thermal properties and hence reduce the reset current [8].

A completely different approach relies on the definition of the contact area between the heater and the GST by the intersection of a thin vertical semi-metallic heater and a trench, called "µtrench"[15], in which the GST is deposited. The µtrench architecture keeps the programming current low and maintains a compact vertical integration. Since the µtrench can be defined by sub-litho techniques and the heater thickness by film deposition, the cell performance can be optimized by tuning the resulting contact area still maintaining a good dimensional control.

5. The Challenges

Since PCM technology is based on the basic properties of the chalcogenide alloy, the integration of the material into a standard CMOS process still represents a challenging matter: not for the single cell concept, already proven to be very strong, but for the manufacturability of very high density NVMs, where the technology can be considered robust only if demonstrated only over many billions of cells.

Another critical topic is represented by the reset current: its controllability and reduction is fundamental to guarantee a compact and scalable cell size, a competitive writing power consumption and enhanced reliability. Hence the development efforts are mainly focus on the optimization of the data-storage structure with respect to the reset current. Recent results have shown good improvements in the cell current reduction with the perspective of a continuous scaling according to the technology node [8, 15].

Considering its key features, the PCM technology is a promising candidate as a mainstream NVM. Although today the technology is still in the early learning curve, the development results and the level of comprehension of the physical mechanisms obtained so far allow foreseeing a fast progress.

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