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GST Confined Structure and Integration of 64Mb PRAM

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Abstract

This paper is focus on the adoption of GST confined structure so as to achieve lower reset current. By modifying to GST confined structure, reset current is down to as small as 0.8mA. Eventually, our integrated 64Mb PRAM based on 0.18μm CMOS technology shows to offer large sensing and reasonable reliability.

1. Introduction

Phase-change Random Access Memory (PRAM), based on the reversible phase-change phenomenon of the chalcogenide, $Ge_2Sb_2Te_5$ (GST) cell, is regarded as a favourite candidate for next generation memory. PRAM covers not only the major merits of current popular memories: DRAM and flash memory [1], such as low cost, high access speed, endurance to cycling and non-volatility, but also other strengths like large sensing signal and great scalability, allowing it be capable of replacing other competitors. Since high reset current is an obstacle of developing high density PRAM, reduction of reset current becomes our key work [2, 3]. Finally, 64Mb PRAM using 0.18μm CMOS technology is fully integrated.

PRAM operates on the reversible high/low resistance of two structural phases. GST material exhibits high resistance as 'reset 1' for amorphous state, as well as, low resistance as 'set 0' for crystalline state. Current pulse is applied to switch reversibly between two states. Fig.1 shows the TEM images of GST cell in reset and set states. In reset state, it is seen that amorphous GST fully covers the contact area with semicircular shape on the top.

2. GST Confined Structure

Reduction of reset current results in smaller cell size, lower power consumption and improved reliability [4]. Apart from controlling the device parameters, 'GST confined structure' is another innovative idea for achieving low reset current. Fig.2 demonstrates the I-V behaviour of PRAM with GST confined cell, indicating 'reset region', 'set region', 'read regime' and 'threshold voltage'.

Fig.3 shows the SEM image of GST confined structure. In this structure, current flows from top electrode contact (TEC) through GST to bottom electrode contact (BEC) via the 'pore'. A part of GST is confined in this small volume. Current distribution in the pore enhances local current density, as well as, joule heating, and thus, reset current is reduced. Fig.4 compares the R-I characteristics of PRAM between normal and GST confined structure. Smaller reset current of 0.8mA is required for GST confined structure.

If we increase the confined GST depth and decrease the contact size, reset current is expected to lower further as the simulation result in Fig.5(a). The reason is that deepening of pore and shrinking of contact size cause longer but smaller current path (i.e. higher BE resistance), reset current is limited. Figures (b) and (c) are simulated temperature profiles of normal and GST confined structure. Obviously, heat loss reduces more efficiently in later structure, and therefore, current density is higher (i.e. I_{reset} is lower).

3. Integration of 64Mb PRAM

64Mb PRAM using 0.18μm CMOS technology is fully integrated. The chip is imaged in Fig.6(a). It is assembled with 128 block units of 512kb sub-array cells. Each block is written by write drivers (W/D) and read by sense-amplifiers (S/A). Fig.6(b) depicts the schematic of 512kb sub-array core architecture with sub-word-line drivers (SWD), S/A's and W/D's. Table 1 illustrates our chip features and process technology. Fig.7 is the TEM image of integrated 64Mb PRAM. Co salicidation and dual work function logic are employed to reduce parasitic resistance and obtain optimal channel resistance. GST cell is placed between TEC and BEC while two metal lines; M0 and M1 are formed as drain line and bit line respectively. Phase-change occurs mainly at the GST-BEC interface.

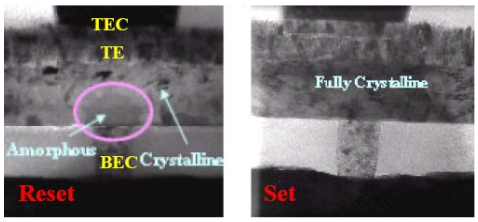
Fig.8 shows the resistance distribution results of reset and set states of 64Mb PRAM cells (R_{reset} ~200kΩ, R_{set} ~2kΩ). The difference between two states is sufficiently large for sensing. In order to confirm the reliability of 64Mb PRAM, some tests are performed. Fig.9 is the endurance test result, ensuring that no fail bit up to 1.58×10^9 cycles. Fig.10 is the data retention test result, revealing that the expected retention time lasts for 2 years at 85°C.

4. Conclusion

At length, 64Mb PRAM based on 0.18μm CMOS technology has been fully integrated and operated. By adopting GST confined structure, reset current is down to 0.8mA. Besides, our integrated 64Mb PRAM has shown to provide good sensing margin and reasonable reliability.

References:

[1] S. Lai and T. Lowrey, *IEDM Tech. Dig.* (2001) pp.803-806
[2] Y. N. Hwang et al., *IEDM Tech Dig. (2003)* pp.893-896
[3] S. H. Lee et al., *Proceedings of VLSI 2004*
[4] T. Lowrey et al., *MRS Fall* (2003) HH2.1



(a) (b)

Fig.1 – TEM images of GST element in (a) amorphous (reset '1') state and (b) crystalline (set '0') state of PRAM

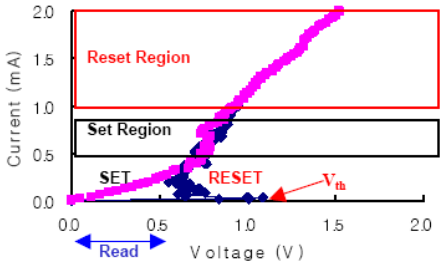


Fig.2 – I-V behaviour of PRAM with GST confined cell

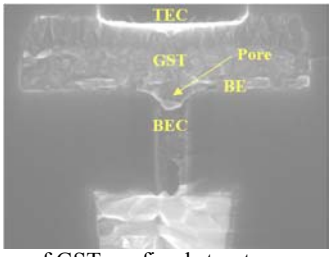


Fig.3 – SEM image of GST confined structure

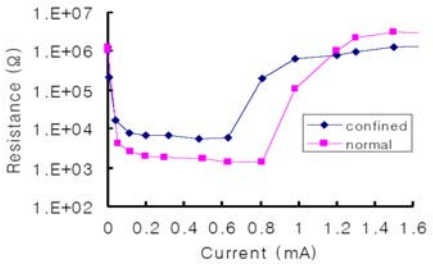


Fig.4 – R-I characteristics of PRAM with GST confined and normal structure.

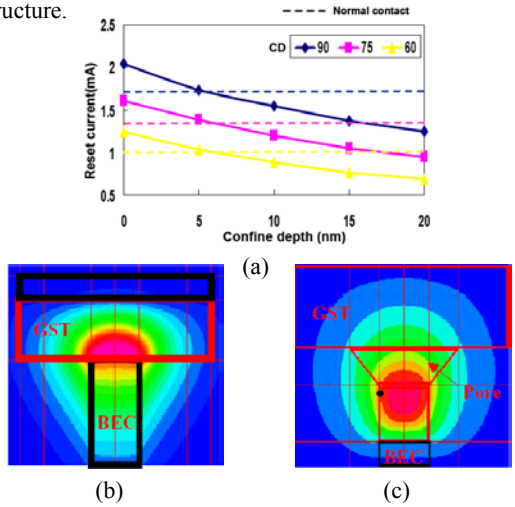
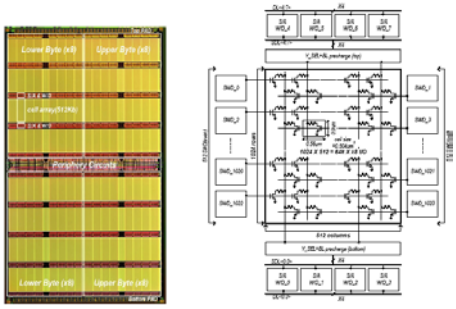


Fig.5 – Simulation results (a) reset current vs. confined depth with varying contact size; temperature profiles of (b) normal and (c) GST confined structure



(a) (b)

Fig.6 (a) Chip image of integrated 64Mb PRAM and (b) schematic drawing of 512kb sub-array core architecture including common shared SWD, S/A and W/D

Organization	4Mb X 16 = 64Mb
Design rule	0.18μm
Supply voltage	3.0V
Chip size	6240μm X 11040μm = 70mm2
Read/Set/Reset time	60ns/100ns/60ns @ 3.0V, 30°C
Material	$Ge_2Sb_2Te_5$ based
Cell size	0.560μm X 0.900μm = 0.504μm2
CMOS technology	Gox=35Å, Dual poly-Si, Co-salicidation
Interconnection	Triple metal (1W-damascene, 2Al)

Table 1 – Summary of 64Mb PRAM chip features and process technology

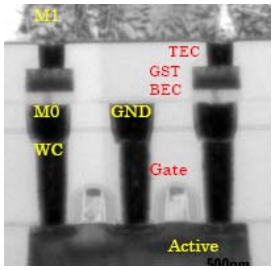


Fig.7 – TEM image of integrated 64Mb PRAM

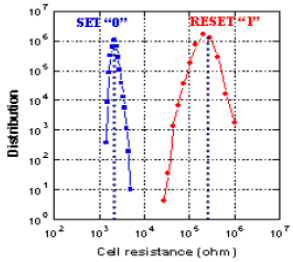


Fig.8 – Resistance distributions of set and reset states of 64Mb PRAM cells (R_{reset} ~200kΩ, R_{set} ~2kΩ)

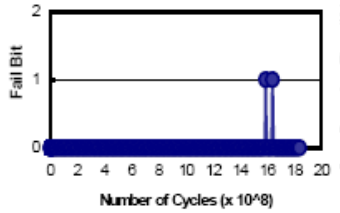


Fig.9 – Endurance test shows no fail bit up to 1.58 X 10^9 cycles

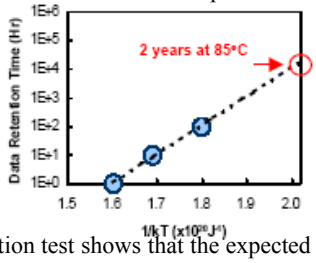


Fig.10 – Data retention test shows that the expected retention time lasts for 2 years at 85°C