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Future Trends in NAND-Type Flash Memory

Riichiro Shirota

Flash Business Strategy Development, Memory Division,

Semiconductor Company, Toshiba Corporation

1- 1, Shibaura 1-Choume, Minato-ku, Tokyo 105-8001, Japan

Tel; 3-3457-3362, Fax; 3-5444-9338, riichiro.shirota@toshiba.co.jp

1.Intorduction

The NAND Flash has been grown for solid state mass storage applications. With the wide spread of the portable equipment, such as digital still cameras and audio/video fields, the demand for high density and low cost Flash has been dramatically increased. To perform low cost and high density Flash, Toshiba has been developed Multi-level cell as well as a cell size reduction.

2.Cell structure

Fig.1 shows the cross sectional view of the memory cell in the 90nm rule at the right hand side compared with those in the 210～130nm rule. Fig.2 shows TEM cross sectional view of the 90nm rule cell. Floating gate (FG) is completely self-aligned to active area. The coupling ratio between CG(control gate) and FG is obtained by inter-poly ONO layer covering the top and sidewall of the FG. The C/R(coupling ratio between CG and FG) can be adjusted to around 0.6, though the tunnel oxide thickness is about 90A and it is possible to realize 2F BL pitch, because the C/R is adjustable by the length of sidewall of FG. By using this cell structure, cell size becomes $4F^2$ (binary) or $2F^2$ (multi-level) , when WL L/S and BL L/S are made by mimmun feature size. This cell structure can be available to the technology node less than 90nm.

3. Multilevel Technology

Muti-level NAND (2bit/cell) has began to product from the 160nm technology node. When the design rule becomes as small as around 90nm, the Vth modulation between the program verify and the read should be concerned. It is due to the FG-FG coupling between the cell-A and adjacent cells-B which are programmed after programming of cell-A. Figure 3 shows the Vth modulation after adjacent cells (cells with common word line and cells with common bit line) as a function of the FG thickness. Less than 0.25V can be acceptable and it can be achieved in case the FG thickness is controlled less than 160nm.

4. NAND cell scaling

As the gate length of the cell becomes smaller, electrical characteristics might be degraded. One of the main concern will be the lowering of the ON/OFF ratio during read operation. Figure 4 shows the sensing scheme for reading of the NAND cell. The NAND cell array has two select transistors at the both side of the cell string. The leakage current of the unselected NAND cell arrays can be suppressed by select transistor not by memory transistor. Thus ON/OFF ratio of the memory transistor is large enough when it is around 10. Furthermore, memory cell does not exposed sever punch through mode during programming. Thus, NAND cell scaling will be able to further proceed less than 40nm.

Figure 5 shows the trend of the NAND Flash scaling. 4Gbit (binary) and 8Gbit (Multi-level) will be achieved using 70nm technology node.

5. Refernces

1) '03 Sympo. on VLSI Tech. pp.89-90, M.Ichige et al.

2)'04 ISSCC "Memory Circuit Design Forum", K.Sakui

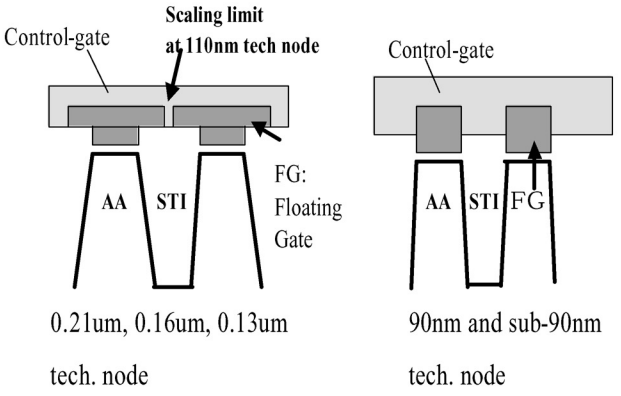

Fig.1 The cross sectional schematic of the cell

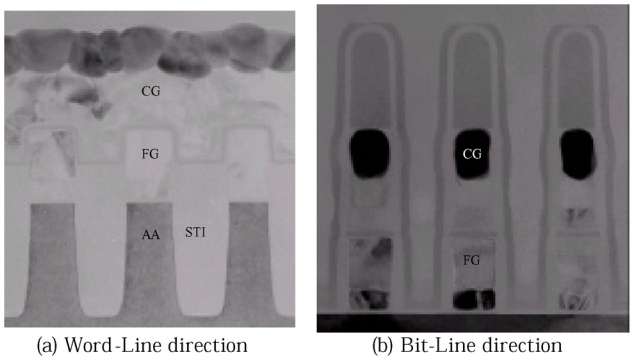

Fig.2 The cross sectional TEM photograph of the 90nm rule cell

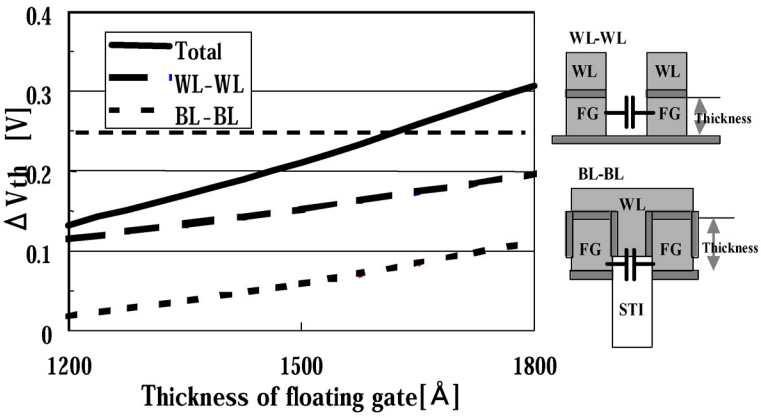

Fig.3 Vt modulation due adjacent cell interference

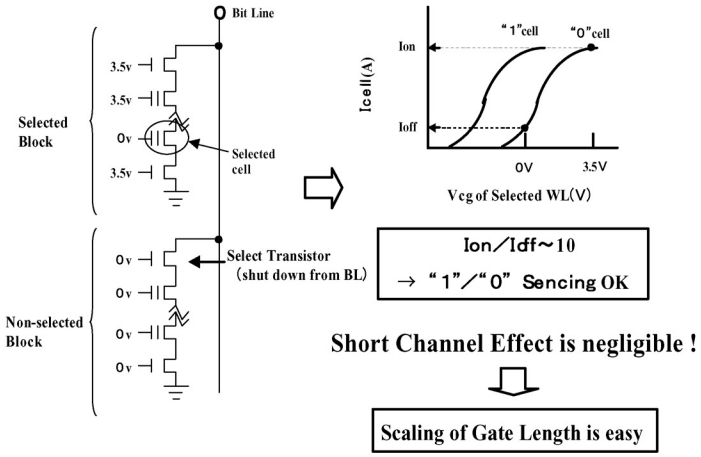

Fig.4 NAND cell sensing scheme for reading

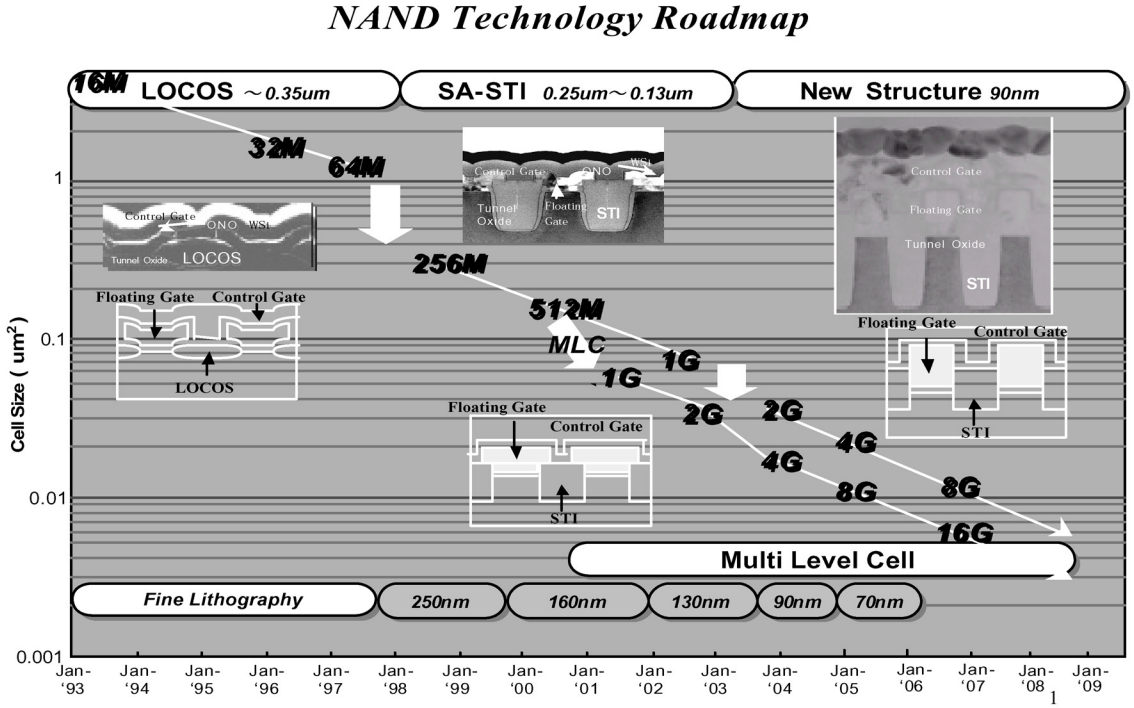

Fig.5 Trend of the cell size scaling