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A Highly Scalable Split-Gate SONOS Flash Memory with Programmable-Pass and Pure-Select Transistors for Sub-90-nm Technology

Yong Kyu Lee, Byung Yong Choi, Jae Sung Sim, Ki Whan Song, Jong Duk Lee and Byung-Gook Park
Donggun Park[1], Chilhee Chung[2]
Inter-university Semiconductor Research Center and School of Electrical Engineering, Seoul National University,
San 56-1, Shinlim-dong, Kwanak-gu, Seoul 151-742, KOREA. Phone: +82-2-880-7279 E-mail: yklee3@snu.ac.kr
[2]C&M, System LSI and [1]Device Research Team, R&D Center, Samsung Electronics Co.
San #24 Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyunggi-Do 449-711, KOREA

Introduction

Since the split-gate type flash memories have relatively higher density than EEPROM and the lower power (low program current) and over-erase free characteristics compared with FLASH, they are applicable to both the mass data storages and stable secure code memories such as SuperFlash [1] and Smart-Cards [2]. Recently, the SONOS flash using charge storage mechanism in the nitride traps have received much attention for their simple structures and high-density applications. In this paper, we introduce a highly scalable split-gate SONOS flash memory. The proposed cell retains many advantages such as low program current, freedom from the over-erase and disturbance. And it is much more scalable than the conventional split-gate flash because it uses a self-aligned gate.

Integration of the Memory Cell

The conventional split-gate cells have an additional control gate (Fig.1(a)) or a deep source junction (Fig.1(b)) to avoid high bias on the select gate. However, the new one has two chargeable nitride nodes under a single gate and shallow S/D junctions as shown in Fig.1(c). Figure 2 shows the cross-sectional SEM image and schematic diagram of the fabricated split-gate flash cell. This split-gate cell consists of three transistor parts, a middle select transistor and two programmable cells at both gate edges. One side charged cell is used for pass cell which can control the current in CHEI (Channel Hot Electron Injection) program mode for the other cell. The middle select cell without programmable node also can remove the over-erase problem even when V_{TH} of the erased cell is negative. We fabricated simple single-gate structure based on the inverted sidewall patterning and gate-damascene process [3]. The gate length and nitride node size are 90-nm and 19-nm, respectively. The final thickness of middle MOSFET is about 10.0-nm and O/N/O layers of both side cells are 3.8/8.5/9.5-nm thick.

Results and Discussion

Figure 3 explains the operation method of the proposed cell as a split gate SONOS flash. At initial mode, pass cell is ready for the program and erase. One of the two nitride nodes is negatively charged to increase the V_{TH} of the pass cell. Such a high V_{TH} of the pass cell has immunity against the punch-through and short channel effect. The program is done by CHEI program and the erase is done by BtBT (Band to Band Tunneling) enhanced HHI (Hot Hole Injection). Figure 4 shows the I_D-V_G characteristics after program and erase. Figure 5(a) shows the program current controllability by manipulating the V_{TH} of the pass cell at the initial mode (simulation result). As the V_{TH} of the pass cell increases, the program current is reduced. As shown in Figure 5(b), the channel potential barrier (Y = 0.005 μm) from the pass cell explains the result of Figure 5(a) well. In spite of the ultra small pass cell gate length (19-nm), the electrically induced channel barrier from the negative charges in the nitride near the source side can effectively control the program current. By virtue of such operation scheme, the gate voltage can be increased high enough to achieve excellent charge injection efficiency at the drain side, retaining a relatively low program current. Figure 6 shows the program speed dependence on V_{DS}. More than 2-V V_{TH} shift within 10 μs can be achieved at the lower drain bias (@V_{DS} < 4 V) mainly due to the short gate length (90-nm) and relatively low tunneling oxide thickness (3.8-nm). From the results of Figure 5 and Figure 6, it is clear that the proposed novel cell has achieved excellent program current controllability and charge injection efficiency simultaneously. Figure 7 shows the over-erase free characteristics due to the middle (select) MOSFET without a charge storage node. Even if the storage node is excessively positively charged, the middle pure MOSFET prevent the final V_{TH} of these serially connected transistors from decreasing into the negative level. Figure 8 shows that thick O/N/O dielectric and non-conducting memory nodes (Si_3N_4) of the new cell can suppress the disturbance from the gate and drain/source. Even after a considerable time has passed, the V_{TH} of unselected cells (programmed or erased) remains almost unchanged.

Conclusions

We proposed and fabricated a highly scalable split-gate SONOS flash based on the modified damascene gate and inverted sidewall process. This new cell shows not only a superior split-gate characteristics even at the 90-nm gate length such as low program current (35μA/cell), immunity to over-erase, and low gate/drain disturbances, but also high performance such as low voltage (V_{DS} < 4 V) operation capability and high program speed (> 2.0 V V_{TH} shift within 10-μs)

Acknowledgements

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References

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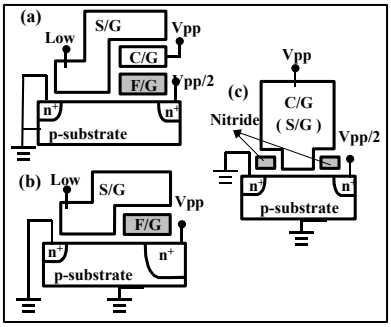


Fig.1 Split-gate flash structures of conventional floating gate (a) triple-gate, (b) source-side injection type, and new (c) SONOS type split-gate

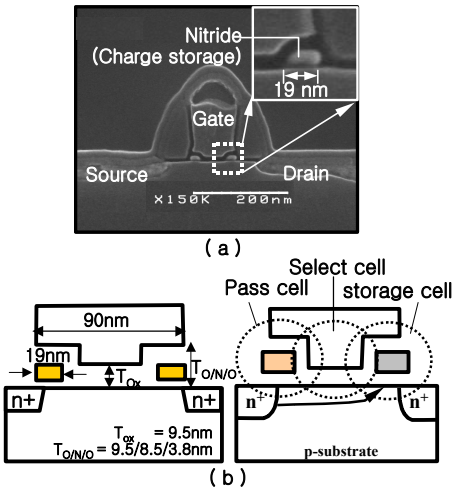


Fig.2 Cross-sectional view: (a) SEM image with self-aligned structure between the gate and storage nitrides (b) schematic diagram. Images of SEM is oxide stained. Thus, Co-silicides on gate and S/D are also stained.

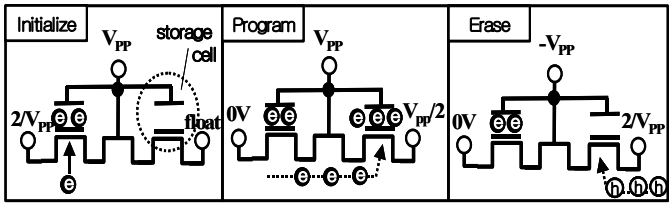


Fig.3 Bias condition for initialization, program and erase. The substrate is grounded.

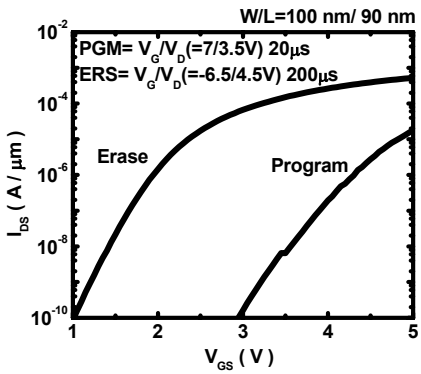
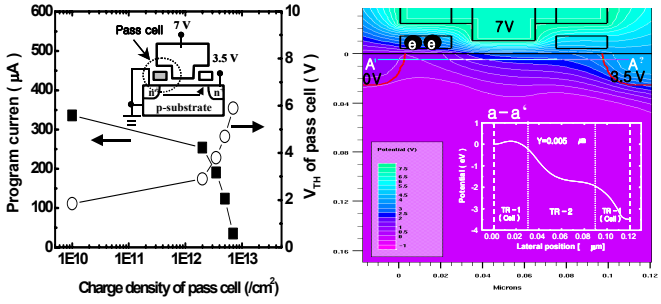


Fig.4 I_D-V_G (@V_S = 1.5 V) characteristics comparison of the split-gate cell after program and erase



(a) (b)

Fig. 5. Simulation results: (a) program current dependence on V_{TH} of pass cell, (b) channel potential contour across A-A' at the program condition (V_{TH} of pass cell = 5.9 V)

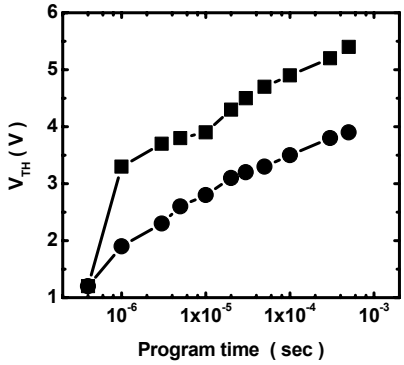


Fig.6 Program speed of split-gate cell; Circle and square symbol marks represent 3V and 4 V V_D , respectively. V_G = 7 V and the others are grounded

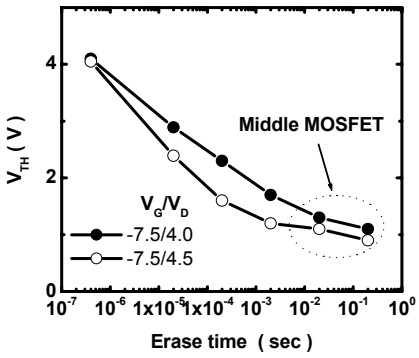


Fig. 7. Over-erase characteristics. V_{TH} is saturated due to the middle (select) MOSFET without a charge storage node.

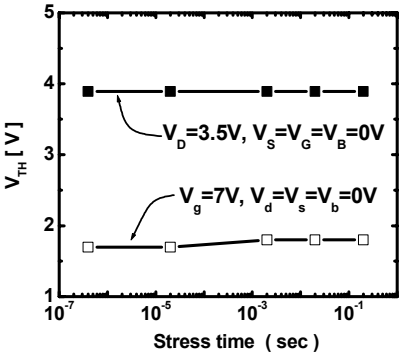


Fig.8 Disturbance from gate and drain for program and erase biasing. Relatively high ONO thickness (3.8/8.5/9.5-nm) suppresses the disturbance.