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Flash EEPROM Tunneling Oxide Reliability Characterization under the test of FN Constant Current Stress and Program/Erase Cycling by using ISSG Nitrided Oxide

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ABSTRACT

In this work, experimental analyses of flash memory nitrided ISSG tunneling oxide reliability under the test of Fowler-Nordheim (FN) constant current stress and memory cell program/erase cycling endurance have been introduced. A correlation between FN constant current stress and program/erase cycling has also been established and verified for the first time and the prediction of the performance of cycling could also be realized.

INTRODUCTION

Considering the NAND flash memory tunneling oxide degradation phenomenon such as the shift of threshold voltage (V_T), the reduction of transconductance (Gm), the distortion of subthreshold swing (S.S.), the increase of SILC (stress induced leakage current) and finally the breakdown of tunneling oxide, the nitrided oxide technology becomes more and more important for improving the reliability of NAND flash memory [1][2].

In this study, ISSG with nitrided oxide reliability was tested by FN constant current stress and program/erase cycling endurance for the first time to monitor the tunneling oxide reliability.

EXPERIMENT

Different tunneling oxide approaches applied on p-well region are listed in Table1 where the oxide thicknesses were fitted by the FN current curves. As shown in Fig.1 (a) and 1(b), there are two devices used in our experiment, one is stacked gate structure, the other is dummy gate structure with a short contact between control gate and floating gate.

RESULTS AND DISCUSSIONS

Part 1. Experimental Results for FN CCS

Fig. 2 (a) Threshold voltage shifts under gate injection for various tunneling oxide recipes and Fig. 2(b) shows I_D-V_G curves (V_D=0.1V) comparison of Dry+N2O and ISSG+10%NO after FN CCS. Positive charge built-up in the oxide dominates the shift of threshold voltage at low charge injected region but negative charge prevails at a higher charge injected region. It is clear that $G_{m,max}$ degradation of ISSG+10%NO is less than others from 0.01 to 0.1C/cm^2 shown in Fig. 3(a) and 3(b).

Trapped-oxide voltage shift and interface trap voltage shift of Dry+N2O and ISSG+10%NO (solid curves means ISSG+10%NO) have been separated as shown in Fig. 4. The positive value of interface trap voltage shift indicates an increase of acceptor-like interface states. The negative value of trapped-oxide charge voltage shift at low injected charge indicates hole trap dominates at low charge fluence but the saturation owed by dominant negative trapped oxide charge at high charge fluence. ISSG+10%NO (solid curves) generates less positive oxide trap than other recipes from the range of 0.01 to 0.1 C/cm^2. Interface trap density keeps increasing with increasing stress and nearly follows the same trend, but ISSG+10%NO generates less interface trap between 0.01 and 0.5 charge fluence compared to others. For example, N_{it} of ISSG, ISSG+ 5%NO and Dry+N_2O are twice as large as ISSG+ 10%NO at the point of 0.05 C/ cm^2 as shown in Fig. 5(b).

Part 2. Program/Erase Cycling Results - Endurance

Fig. 6 shows program/erase cycling characteristics for various tunneling oxide recipes. It is obvious that ISSG+10%NO (solid lines) shows the best performance of 10^4 program/erase cycles, threshold voltage shifts of about 1V, 1.2V, 0.25V and 0.9V, therefore ISSG+10% NO does enhance the endurance of flash memory cells compared to others. Fig. 7 shows less degradation ofcell current at 0V gate voltage after program/erase cycles for ISSG+10%NO, which is consistent with the previous measured data. I_D-V_G curves of stacked-gate cell transistor after 100K (10^5) program/erase cycles were measured as shown in Fig. 8. Regardless of the shift caused by oxide trapped charge, S.S. distortion of ISSG+10%NO is the least serious among all tunneling oxide recipes, which means interface generation rate is lower than others.

MODELING AND CONCLUSION

The charge fluence through the tunneling oxide under FN constant current stress can be extracted from program/erase cycle window (threshold voltage window) and the number of cycles the memory cell has endured. If we assume the threshold voltage window of program and erase cycling is 3.5V (= 2V-(-1.5V)), ONO capacitance is about $7.52\times10^{-7}\,F/cm^2$ due to the effective oxide thickness of an oxide-nitride-oxide (ONO) inter-polystack is 14nm. Therefore, the charge fluence for each program/erase cycle is about $2.63\times10^{-6}\,C/cm^2$. The charge fluence at 10K program/ erase cycle is about 0.0263 C/cm^2 and those at 100K program/erase cycle is about 0.263 C/cm^2.

From Fig. 5(a) and 5(b), we observe that ISSG with 10% NO annealing prevails over other recipes not only in trapped-oxide charge but in interface trap charge density at the point from 0.01 to 0.1 C/cm^2, which quite correlates with program/erase cycling characteristics as shown in Fig. 6(a) and 6(b).

Many researchers have reported that electron-hole pairs are generated at the anode during FN current injection and the generated holes are injected back into the tunneling oxide, generating the hole traps at the same time [6]. It was also proposed that neutral electron traps are created by the energy released through the recombination of electrons and holes, which is the mechanism of electron-trap generation during FN constant current stress. The origin or generation mechanism of interface trap is still controversial but the most acceptable reason is hydrogen related model. The main idea of this model is the recombination of a trapped hole and a free tunneling electron and the event occurs near the Si/SiO_2 interface. The recombination event may either directly or indirectly release hydrogen from a passivated interface state [6][7].

According to the electron trap and interface trap generation mechanism mentioned before, trapped-hole in the tunneling oxide plays an important role. In other words, if fewer holes trapped in the oxide, less oxide-trapped charge and less interface trap will be generated accordingly. And the reported source of trapped hole is E' center which is capable of trapping hole. The mechanism of producing an E' precursor is oxygen outdiffusion from the oxide with accompanying diffusion into the substrate or poly-Si in the form of oxygen interstitials. The outdiffusion driving force mainly comes from Gibbs free energy. The maximum reduction of this energy occurs at the interface between the nitrided oxide and Si substrate in our case. Therefore, it is not easy to produce an E' center precursor near the interface of SiO_2 and Si since the nitrogen atoms are preferentially distributed there [7].

From the aforementioned data, superior tunneling oxide reliability can be obtained from ISSG+10%NO.

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Table 1. Conditions of nitrided oxide formation and physical parameters				
Sample	ISSG	ISSG + 5% NO	ISSG + 10% NO	Dry + N2O
Nitridation temperatures	NA	950C	950C	800C
Electrical oxide thickness	8.7nm	8.7nm	8.7nm	8.2nm

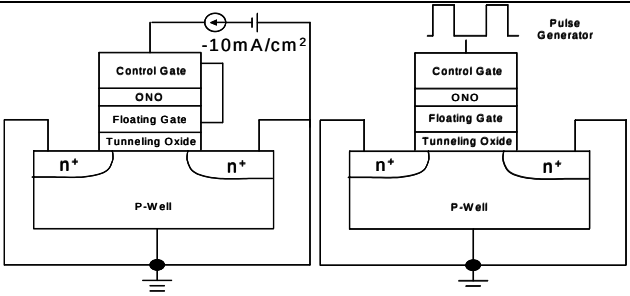


Fig. 1(a) Fig. 1(b)

Fig.1 Schematic diagram of the flash EEPROM and experimental setup for (a) the test of FN Constant Current Stress (FN CCS) (b)the test of program/erase cycling endurance.

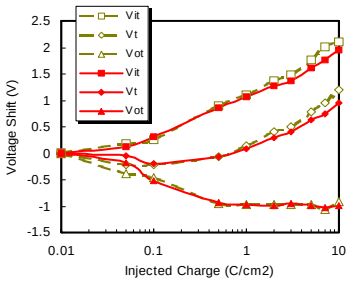
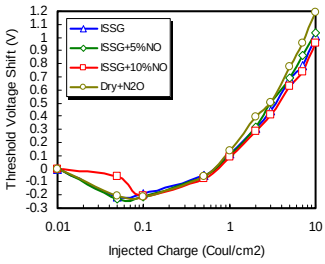


Fig. 4 Threshold voltage shift and its separation of trapped-oxide charge and interface trap charge voltage shift under gate injection stress.



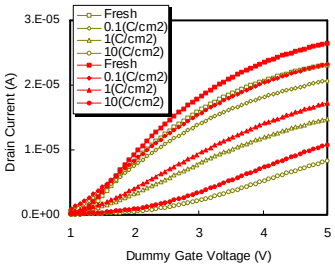


Fig. 2(a) Fig. 2(b)

Fig. 2 (a) Threshold voltage shifts under gate injection for various tunneling oxide recipes. Their initial V_T values are nearly the same at 1.2V (b) I_D-V_G curves (V_D=0.1V) comparison of Dry+N2O and ISSG+10%NO after FN CCS.

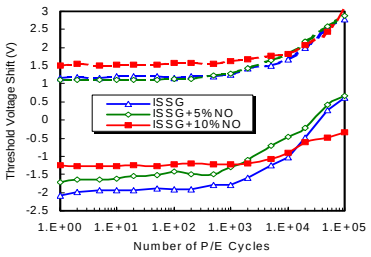
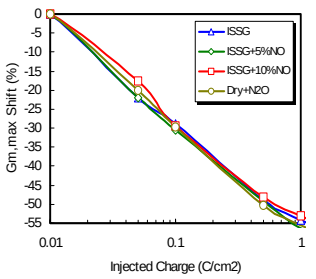


Fig. 6(a)



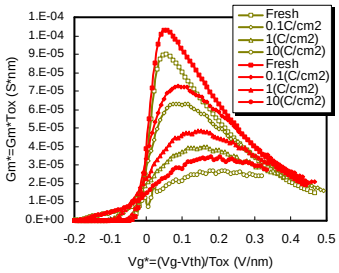


Fig. 3(a) Fig. 3(b)

Fig. 3 (a) The maximum transconductance shift (%), the initial G_m maximum values of ISSG, ISSG+5%NO, ISSG+10%NO and Dry+N2O are 1.2E-5, 1.2E-5, 1.2E-5 and 1.1E-5 respectively; (b) normalized G_m of Dry+N2O and ISSG+10%NO.

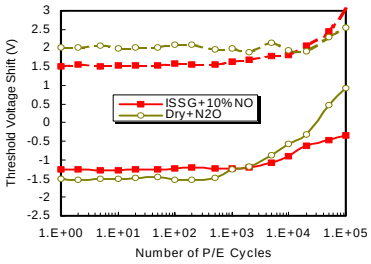
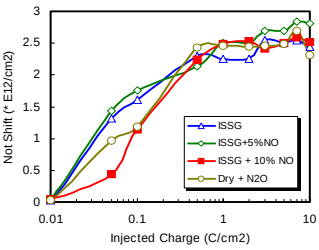


Fig. 6(b)

Fig. 6 P/E cycling characteristics which were tested under the same initial tunneling electric field.



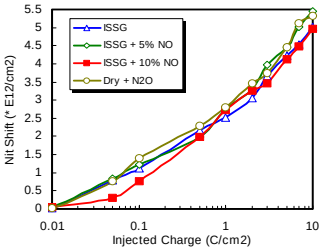


Fig. 5(a) Fig. 5(b)

Fig. 5(a) The shifts of oxide-trapped charge density, Fig. 5(b) The shifts of interface trap density.

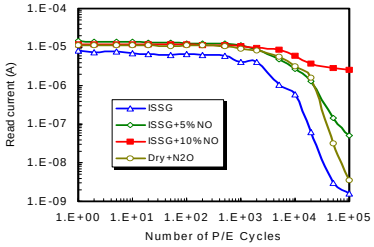


Fig. 7 Cell read current judged by the values of drain current at the fixed gate voltage (V_G=0V).

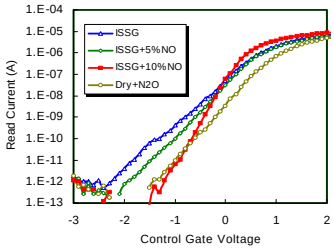


Fig. 8 I_D-V_G curves of the stacked-gate cell transistor characteristics after 100K program/erase cycling for the programed cell (low threshold voltage).