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Impact of Co-salicide capping layer on GIDL in High Voltage devices for Embedded Flash memory

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Introduction

Self-aligned $CoSi_2$ has been widely employed for its immunity to narrow line width effect and good thermal stability for sub-micron high performance CMOS logic devices [1]. However, to minimize the junction leakage of Co salicide process becomes more and more critical for shallow junctions with scaling down of device size, especially for Flash memory products. Flash memory requires high voltage devices to generate higher voltage than the standard supply voltage (Vdd) for correct programming and erase operation [2-3]. So far, many studies have been done to reduce the junction leakage of Co salicide process, as well as mechanism study, but most of them mainly focused on logic circuits that can be supported by standard Vdd [4-5]. Moreover, some works have been carried out to investigate the capping layer's effect of the $CoSi_2$ formation on the barrier property and the reaction rate control of Ti or TiN capping layer [6-7], the advantages of each capping layer were also discussed. In this study, we discussed the effect of Co salicide capping layer on Gate-Induced Drain Leakage (GIDL) current for high voltage devices, which generate the high voltage for flash memory cell array. It is first time reported that Ti-incorporating capping layer may reduce GIDL current of high voltage device dramatically by comparing with the pure TiN-capping layer. In particular, the optimal capping layer (Ti-rich TiN) with the advantages of both Ti and TiN film to suppress GIDL current on high voltage devices has been proposed, which keeps a good junction leakage and salicide contact resistance (Rc), concurrently.

Experimental

All the devices studied in this work were fabricated using a 0.15um emmbedded Flash memory technology with shallow trench isolation (STI). After the high voltage transistors with a thick gate oxide were formed, a conventional Co salicide process has been carried out with splits on different capping layers, including TiN, Ti and Ti-rich TiN layers as illustrated in Fig.1. After full process integration for each split, n+/p junction leakage, GIDL and salicide Rc across a wafer for each split have been measured, in order to understand the effect of capping layer. High voltage nMOS, with a gate oxide thickness of ~20nm and W/L=0.50um/1.0um is used for this measurement, as it is typically used in the actual charge pump and decoder system in Flash memory as shown in Fig.2. In addition, two devices with different salicide protection over etch times were fabricated to examine the effect of Si-interface contamination on GIDL using Co/TiN film.

Results and Discussion

In order to program and erase flash memory, high voltages are needed to make the Fowler-Nordheim tunneling effect in flash memory cell. Normally, different high voltages are generated on board of flash memory, which request less power consumption and overall leakage on high voltage transistors has to be minimized [3]. In our work, junction leakage current of high voltage nMOS was evaluated on different Co salicide capping layers as presented in Fig. 3, devices with Ti or Ti-rich TiN capping layers show 2 order lower leakage current and better uniformity at a given bias condition (Vd=12V, Vg=Vs=Vsub=0V), by comparing to TiN capping layer. As shown in Fig.4 (a) and (b), I-V measurement, the leakage difference between different capping layers is mainly from GIDL component. The high leakage current (GIDL component) for the device with TiN capping layer can be clearly observed at Vd > 8V, whereas no such high GIDL current for devices with Ti-rich TiN capping layer. As we know, if we bias the drain from 0V to 12V with Vg=0V, both junction leakage and GIDL current are measured in Fig 4. (a). But the junction leakage only can be monitored at Vd=0~12V with gate floating on devices as shown in Fig.4 (b). GIDL component can be derived by substracting (b) from (a) easily [8], which indicating the abnormal GIDL for TiN capping layer. It is believed that GIDL difference between TiN and Ti (or Ti-rich TiN) capping layers is due to the different Si-interface contamination beneath $CoSi_2$ salicide film, in terms of oxygen contamination or unwanted oxide residue at the edge of nitride spacer as represented in Fig.5. This Si-interface contamination can be influenced by the previous processing steps such as spacer etch and the subsequent surface cleaning process, eventually, it acts as the driving force to enhance electric field and increase GIDL at the edge of nitride spacer within wider depletion region under high enough voltage application on the high voltage transistors. The incorporating Ti at the deposition stage react with the existing interfacial oxide [9], results in reducing unwanted oxide or oxygen contaminations, and causes the decrease of GIDL current under a critically higher electric field between gate and drain terminals (potential difference between gate and drain > 8V, but no leakage difference at < 8V).

To verify this effect of Si-interface contamination on GIDL current, we fabricated two high voltage devices with different salicide protection over etch (O/E) splits, including nominal O/E split 1 and intentionally increased O/E by 20% split 2, to make sure that Si-interface is completely clean prior to Co/TiN film deposition in Fig. 6. The results show that GIDL current of the device with split 2 is reduced by ~2 order comparing with split 1. Moreover, TEM image in Fig. 7 reveals a thicker Co salicide layer for the device with split 2, increased O/E split. As a result, we found out that the Si-interface contaminations prior to Co deposition at the edge of nitride spacer causes GIDL current to increase abnormally at a critical high electric field between gate and drain regions. In addition, we also confirmed that TiN or Ti-rich TiN capping layers have lower salicide N+ Rc, comparing to Ti capping layer (Fig.8) as reported in some other study [7]. At the same time, TiN-capping layer also shows much more tailing for logic transistor related junction leakage by comparing Ti or Ti-rich TiN capping layers as shown in Fig. 9. Therefore, Ti-rich TiN film is a very promising candidate as Co salicide capping layer, which effectively suppress GIDL current on high voltage devices, and still keeping a good junction leakage and salicide N+ Rc, comparing to conventional Ti or TiN capping layers.

Conclusion

We have studied the impact of Co salicide capping layer on high voltage nMOS devices in 0.15um embedded Flash memory product. Experimental results indicate that by incorporating Ti into Co film, the GIDL current is significantly reduced for the same level of interfacial contamination. A new Ti-rich TiN film as Co salicide capping layer has been proposed in our work, which combines the advantages of both Ti and TiN capping layers to suppress the GIDL current on high voltage device in Flash memory.

References

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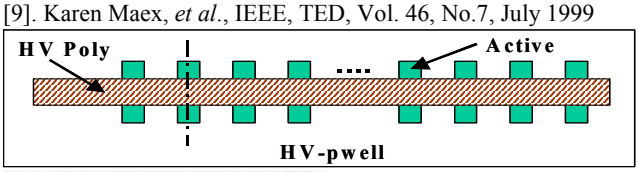
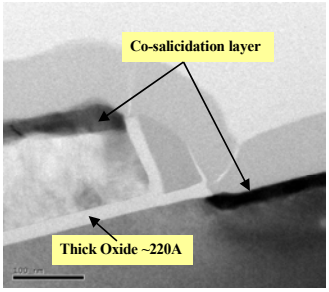




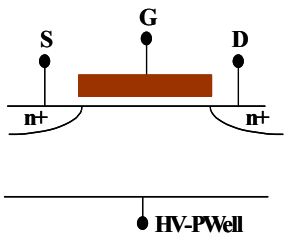


Fig.2 Actual layout and cross-section TEM image for GIDL current evaluation from high voltage nMOS(W/L=0.50/1.0um) transistor which is used for actual charge pump and decoder system in Flash memory product in order to investigate the impact of the differenct capping layers on GIDL current in this study.

- STI
- HV-Well formation
- Gate oxidation (thick~200A)
- HV-Poly formation followed by S/D implantation
- Salicide protection Photo & Etch
- Des-oxidation
- Co-deposition with capping layers → Capping layer splits: A : TiN; B : Ti; C : Ti-rich TiN
- 1st RTA
- Removal of un-reacted layers
- 2nd RTA
- SiN deposition
- ILD
- Contact and metallization

Fig.1. Key process flow with several capping layer splits for this experimental work.

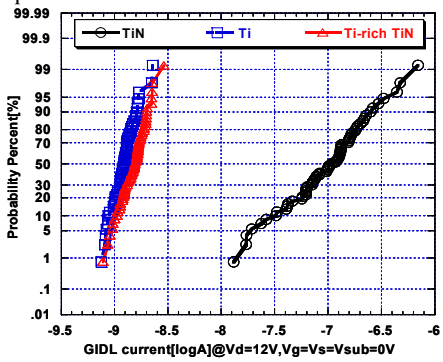
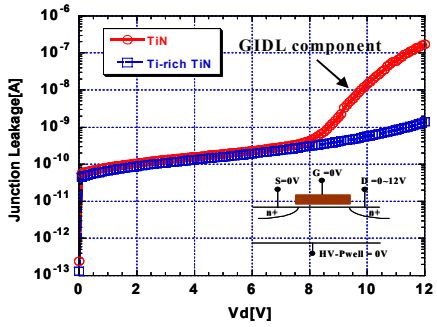
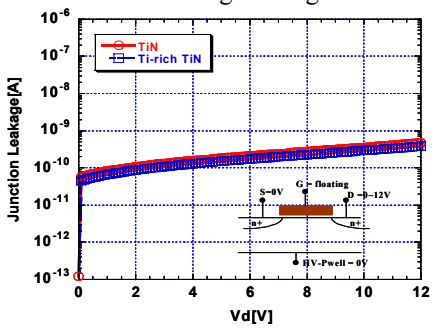


Fig.3 Probability of junction leakage (mainly GIDL current) on high voltage nMOS for different Co-salicide capping layers.



(a) Junction leakage + GIDL current



(b) Junction leakage only

Fig. 4 Both junction leakage and GIDL current (a) are measured at Gate=0V, and junction leakage only (b) is monitored at Gate=Floating on both TiN and Ti-rich TiN capping layers using high voltage nMOS transistor. GIDL component from high voltage device with TiN capping layer can be clearly observed at Vd > 8V, whereas no GIDL current for that with Ti-rich TiN capping layer as seen in the figure (a).

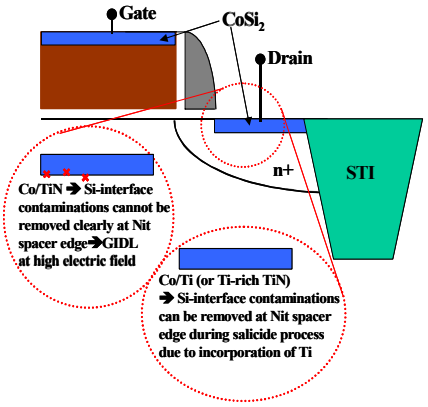
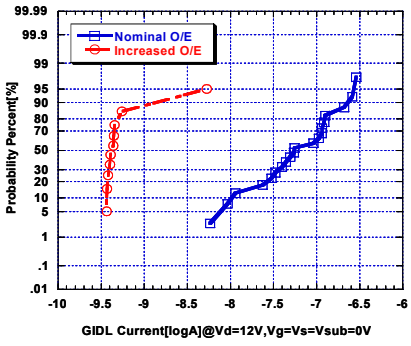
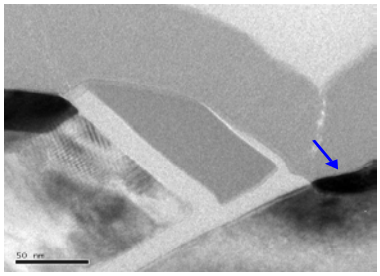


Fig.5 Schemetic illustration of the relationship bwtween GIDL and Co-salicide capping layers.

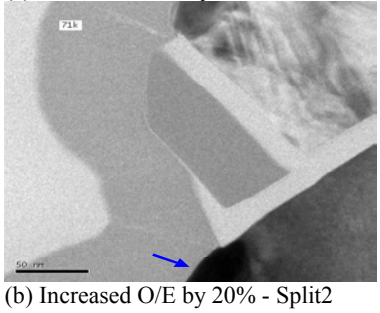


- Salicide protection Photo & Over etch(O/E) split
  - Nominal –split 1
  - Increased by 20% - split 2

Fig.6 Probability percent of GIDL on high voltage nMOS transistor for salicide protection over etch splits using TiN capping layer.



(a) Nominal O/E – split1



(b) Increased O/E by 20% - Split2

Fig.7 TEM image on $CoSi_2$ thickness for differenct salicide protection O/E split with TiN capping layer.

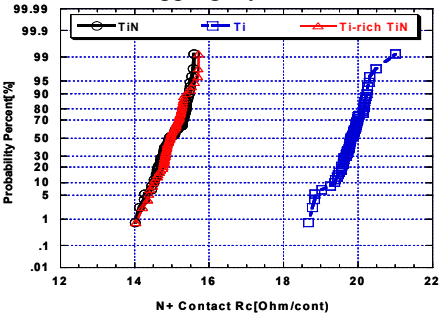


Fig.8 N+ contact resistance for each capping layer.

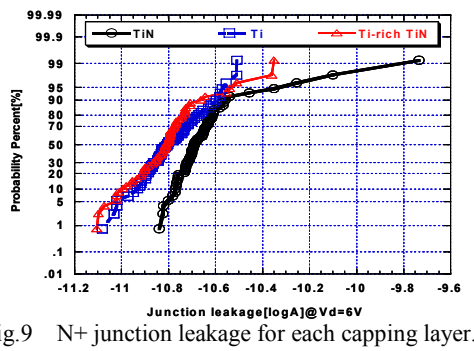


Fig.9 N+ junction leakage for each capping layer.