Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 258-259

D-5-1 (Invited)

Diamond MISFETs for High Frequency Applications

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1. Introduction

The progress of information technology (IT), especially wireless communication system, has dramatically changes our lives. It is believed that the traffic growth will continue for a considerable time in the future. The third generation or newer mobile communication systems that can support the traffic growth, require high power and low distortion power amplifiers based on the development of extremely high power (>300W) RF transistors. Recently, diamond has attractive attentions as one of the materials for high-power and high-frequency devices due to the superior material properties such as a wide band gap (5.45 eV), high breakdown field (>10 MV/cm), maximum thermal conductivity in materials (22 W/cmK), and a low dielectric constant (5.7) [1]. Consequently, figures of merit (FOM) of diamond are extremely high. For example, Johnson's FOM [2] of diamond, which is used for evaluating materials for high-power and high-frequency device applications, is much higher than that of other materials even in wide-gap materials; that is 100, 2.6, 2.5 times of Si, SiC and GaN, respectively.

The surfaces of diamond films deposited by plasma-assisted chemical vapor deposition (PACVD) are terminated by hydrogen. The hydrogen-terminated (H-terminated) surface exhibits p-type conduction without doping impurities such as boron [3]. This H-terminated surface conductive layer is suitable for the channel of field-effect transistors (FETs) because of the following excellent properties. 1) The sheet density of holes is as high as 10^{13} /cm^2, which is comparable to that of the AlGaN/GaN heterostructure. The carrier density is constant in the temperature range from 150 K to 400 K [4] because of the low carrier activation energy of less than 50 meV. 2) The carriers are confined in a thin subsurface region of less than 10 nm thickness [5]. 3) The H-terminated surface exhibits a low density of surface states (less than 10^{11} /cm^2) [6], which might be due to the termination of surface dangling bonds by the hydrogen atoms. Consequently, FETs utilizing H-terminated surface channel shows higher characteristics [7, 8] than impurity doped diamond devices.

In order to improve the performance of FETs not only the reduction of the gate length but the reduction of parasitic resistances, especially source resistance, is important. We have developed a self-aligned gate fabrication process which can reduce the source-gate and gate-drain spacings to less than 0.3 μm. Reduction of these spacings is the effective technique to reduce the parasitic resistances at present. Utilizing the self-aligned gate fabrication process, high performance metal- semiconductor (MES) FETs and metal-insulator- semiconductor (MIS) FETs have been fabricated on the H-terminated diamond surface channel. The RF operation of diamond FETs has also been also realized by utilizing this fabrication process.

2. Experimental

RF diamond FETs were fabricated on homoepitaxial diamond films. The diamond homoepitaxial films were deposited on high-pressure high-temperature synthetic Ib (001) substrates by the PACVD. The source gas was methane diluted by hydrogen ($CH_4/(H_2 + CH_4)$ = 0.1-3 %). The deposition time was 10-3 hrs. The sheet resistance of this substrate was 10-30 kΩ/sq.

The gate length of FETs fabricated by the self-aligned gate process is 0.2-5 μm with the source-gate and gate-drain distance of 0.2-0.3 μm.

3. Results and Discussions

The on-wafer RF characteristics of diamond MISFETs have been measured. Figure 1 shows the typical RF gains of diamond MISFETs. The gate length of the MISFET is 0.2 μm. The cut-off frequency and the maximum frequency of oscillation of the diamond MISFET are 22 and 25 GHz, respectively. More than 15 dB of power gain (MSG) is obtained at 2 GHz operation frequency. These values are comparable to the maximum values of SiC MESFETs.

Figure 2 shows the cut-off frequency as a function of reciprocal gate length for diamond MES (NTT&Ulm Univ. [9]) and MISFETs, GaN HEMTs, and SiC MESFETs. Saturation carrier velocities of 10^7, $5x10^6$ and 10^6 cm/s

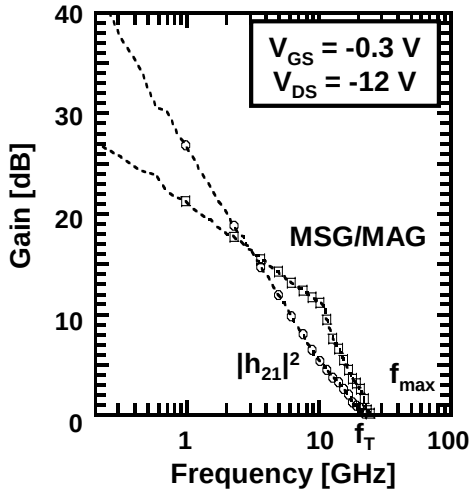

Figure 1. RF gains of 0.2 μm gate diamond MISFET.

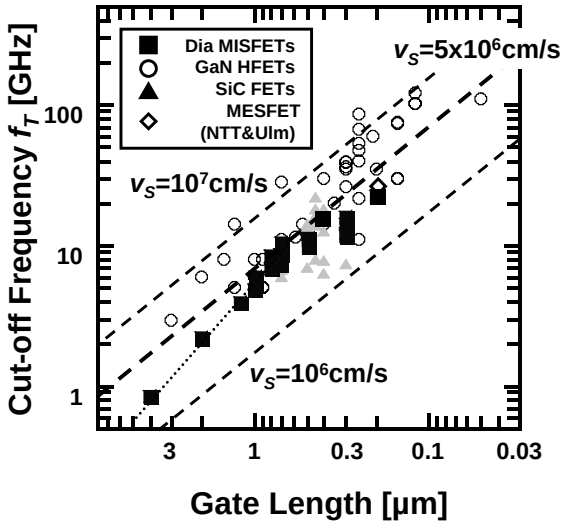

Figure 2. Cut-off frequency of diamond, GaN, SiC transistors as a function of the gate length.

from the equation of $v_S=2\pi f_T L_G$ are illustrated. The cut-off frequency of GaN HEMTs increases with the reduction of gate length according to the $1/L_G$ law and the saturation velocity is distributed from $5x10^6$ to 10^7 cm/s; those values are 1/2-1/4 of the saturation velocity of bulk GaN. The cut-off frequencies of diamond MISFETs also increase with the reduction of the gate length. In particular, when the gate length is longer than 0.7 μm, the cut-off frequency improves further than that predicted on the basis of the inverse gate length law because of the comparatively low mobility of H-terminated surface channel. Accordingly, the transconductance increases with the reduction of the gate length even at the submicron gate length. On the other hand, RF characteristics of diamond FETs with deep sub-micron gate length deviate from the characteristics improvement trend with the carrier velocity of $5x10^6$ cm/s. One of the reasons of the degradation from the trend is the parasitic resistance and capacitances. As mentioned above with the DC characteristics, effects of source resistance can not be negligible in deep sub-micron devices despite narrow source-gate spacing of 0.2-0.3 μm. The parasitic coupling capacitances between source/gate and gate/drain electrodes are also considerable in this device. From our estimation using 3D electromagnetic simulation, the coupling capacitance between gate and drain electrodes becomes more than 15 % of gate-drain capacitance C_{GD}.

As shown in fig. 1, the maximum frequency of oscillation is low compared with cut-off frequency due to the low power gain (MAG) in high frequency. The typical f_{max}/f_T ratio of 0.2 μm diamond MISFETs is 1.1-1.5. This f_{max}/f_T ratio decreases along with the reduction of the gate length. As mentioned above this low power gain is due to the parasitics, especially source, gate and drain resistances, gate-drain and source-drain capacitances. In order to improve the f_{max} and realize the high power with stable operation in diamond FETs, development of new device fabrication technology is required. Required device technology is summarized in fig. 3. Reduction of the gate resistivity is

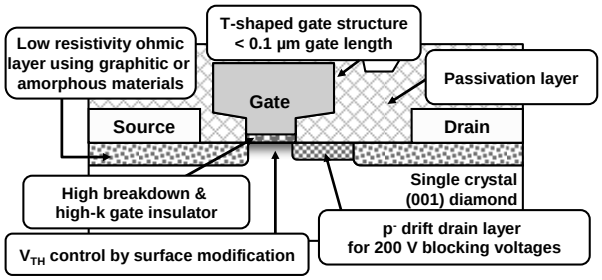

Figure 3. Required device fabrication technology for high power diamond RF transistor.

realized by adopting the T-shaped gate structure. By utilizing T-shaped gate structure, gate resistance is highly decreased from 100 [10] to 20 Ω in 0.2 μm MISFET. Consequently, the f_{max}/f_T ratio has been improved from 1.1 to 2. Low ohmic resistance (source and drain resistance) is realized by utilizing graphite or carbide layer, those are obtained by Ni ion irradiation. Partially channel oxidization technique can control the threshold voltages and normally-off diamond MISFET will be realized. When we adopt the p^- drift layer in drain region, more than 200 V of breakdown voltage will be realized. Accordingly more than 10 W/mm of saturation power is expected in this new device structure.

Acknowledgements

This work is supported by a grant of NEDO (New Energy and Industrial Technology Development Organization) and also in part by a Grant-in-Aid for Center of Excellence (COE) Research from the Ministry of Education, Culture, Sports, Science and Technology and by the Advanced Research Institute for Science and Engineering, Waseda University.

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