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**Source resistance reduction of AlGaIn/GaN HFET using novel superlattice cap layer**

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Phone: +81-75-956-9083 Fax: +81-75-956-9110 E-mail: [murata.t@jp.panasonic.com](mailto:murata.t@jp.panasonic.com)**1. Introduction**

AlGaIn/GaN HFETs are drawing considerable attention not only as high power RF devices [1] but also as small signal amplifiers or as RF switches [2]. One emerging issue of these devices is their high parasitic, i.e. source and ohmic contact, resistances resulting in seemingly low transconductance. One promising approach to overcome this problem is to cap the AlGaIn barrier layer with a highly doped n-type GaN layer. Although a remarkable improvement in transconductance with this technique has been reported [3], mechanism leading to such a performance is not clear and a definite methodology to reduce the parasitic resistance in AlGaIn/GaN HFETs has not been established yet. In this respect, an AlGaIn/GaN superlattice (SL) capped structure is another very attractive technique in which dramatic increase of electron density is expected owing to the existence of the multiple AlGaIn/GaN interfaces in the SL cap. In this work, we have demonstrated for the first time, an excellent performance of the SL cap which significantly reduced the parasitic effects. Correspondingly, we confirm increases of the drain current and the transconductance with the SL cap by 13%. Detailed calculation results show that the primary functions of the SL cap are two folds: (1) Lowering of the effective barrier height seen between the contact metal and the 2 dimensional electron gas (2DEG). (2) Lowering of the sheet resistance due to the increased charge concentration within the SL layer. It is noted that a remarkable, i.e. 75%, reduction of source resistance is achieved with this technique compared with the GaN cap method.

**2. Principle of source resistance reduction by the SL cap**

A basic structure of SL capped HFET is illustrated in Fig.1. The source and drain ohmic electrodes are formed on the SL cap layer while the gate electrode is formed on the original HFET barrier layer surface. Because of the existence of the multiple AlGaIn/GaN interfaces, electron density in the SL cap is expected to be high. In Fig.2, conduction band energy levels of an SL (solid line) and a GaN (dotted line) cap structures calculated by a self-consistent Poisson-Schrödinger equation solver. It is clearly seen that the effective potential barrier ( $\phi_{\text{AlGaIn}}$ ) between the surface Fermi level and the top of the conduction band of the AlGaIn barrier is lowered by 0.5 eV for the SL cap layer.

**3. Experimental Procedure**

The layer used in this study was grown by metal-organic chemical vapor deposition (MOCVD). The structure of the SL capped AlGaIn/GaN HFETs consisted of  $n^+$ -GaN/ $n$ -AlGaIn/ $n$ -GaN SL/ $n$ -AlGaIn/ $i$ -GaN/AlN buffer/Sapphire substrate as illustrated in Fig.1. The SL layers were doped with Si and the concentration was  $1 \times 10^{19} \text{ cm}^{-3}$ . The total thickness of the SL layers was constant, i.e. 50nm. Several

types of the SL caps were prepared by the ratio of thicknesses of AlGaIn and GaN layers. As a reference, we fabricated an n-GaN capped HFET.

Source/drain and gate electrodes were Ti/Al and PdSi/Pd/Au, respectively. Gate electrodes with 1  $\mu\text{m}$  length were formed on the AlGaIn barrier layer after recessing the cap layers.

The source resistance and the ohmic contact resistance of the fabricated HFETs were measured by the Yang-Long [4] and the transmission line model methods, respectively.

**4. Results and Discussion**

In Fig.3, transmission electron microscope (TEM) image of an SL cap is shown. Excellent quality of the layer is confirmed by the sharp AlGaIn/GaN interfaces, by thickness uniformity of each layer, and by high crystallinity. Figure 4 shows DC characteristics ( $I_D$ - $V_D$  curves) of the fabricated HFETs with the SL and the GaN caps. It is obvious that the drain current of the SL cap HFET increased by about 13% as compared to that of the GaN cap HFET. Also, the low field on state resistance of the SL cap HFET is lower than that of the GaN cap device as indicated by the large difference in the slopes of the two  $I_D$  curves. Correspondingly, transconductance in saturation regime of the SL cap HFET also improved by 20% as shown in Fig. 5.

The measured source ( $R_s$ ) and contact ( $\rho_c$ ) resistances of each device are tabulated in Table 1. It is interesting to observe that both  $\rho_c$  and  $R_s$  are strong functions of the AlGaIn/GaN thickness ratio within the SL layer: With the increase of the relative AlGaIn thickness, the  $R_s$  and  $\rho_c$  were found to be minimized to 1.0  $\Omega\cdot\text{mm}$  and  $1.1 \times 10^{-5} \Omega\cdot\text{cm}^2$ . The electrical properties of the capped HFET structure can be analyzed by the Feurer's 2-layer model shown in Fig.6 [5]. With this model, the total resistance between points A and B can be analytically expressed. Since the sheet resistances of the cap ( $r_{s1}$ ) and 2DEG layers ( $r_{s2}$ ), the contact resistance between source and the cap ( $R_{c1}$ ) and the total resistance between point A and B ( $\rho_c$ ) can be determined experimentally, the only unknown resistance of  $\rho_{12}$  is uniquely determined. In Table 1, thus obtained  $\rho_{12}$  are tabulated. It is interesting to observe that  $\rho_{12}$  and  $R_s$  have strong correlation. Furthermore, in Fig.7, we plot the effective barrier height,  $\phi_{\text{AlGaIn}}$  calculated by the above-described calculation shown in Fig.2 and the extracted  $\rho_{12}$  of each sample. It is confirmed that the two quantities are linearly proportional suggesting that the effective barrier lowering is indeed due to the effective tunneling barrier decrease in addition to the sheet resistance lowering.

**5. Conclusion**

We have demonstrated a new method to reduce the parasitic resistances of AlGaIn/GaN HFETs by the SL cap structure for the first time. It was shown that the SL cap is capable of lowering of the effective barrier height seen

from the contact metal to 2DEGs. It was confirmed that the drain current and the transconductance with the SL cap were increased by 13% and 20%, respectively. We emphasize that the SL cap is indeed a versatile tool to engineer the parasitic effect of the AlGaIn/GaN HFETs.

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### References

[1] K.Joshin, T. Kikkawa, H. Hayashi, T. Maniwa, S.

Yokokawa, M. Yokoyama, N. Adachi and M. Takikawa, IEDM 2003 tech. digest pp983-985 (2003).

[2] H. Ishida, Y. Hirose, T. Murata, A. Kanda, Y. Ikeda, T. Matsuno, K. Inoue, Y. Uemoto, T. Tanaka and D. Ueda, IEDM 2003 tech. digest pp583-586 (2003).

[3] H.Okita, K. Kaifu, J. Mita, T. Yamada, Y. Sano, H. Ishikawa, T. Egawa and T. Jimbo, Phys. stat. sol. (a) 200, No.1, pp187-190 (2003).

[4] L. Yang and S. I. Long, IEEE Electron Devide Lett. EDL-7, No.2 (1986)

[5] M. D. Feuer, IEEE trans. Elect. Dev. ED-32, No.1 pp7-11 (1985)

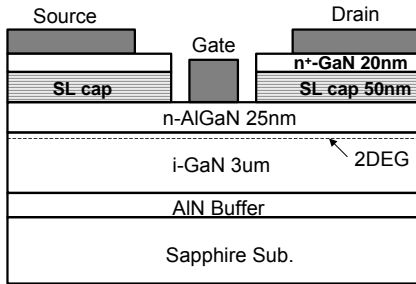


Fig. 1 A cross sectional view of a fabricated SL cap HFET.

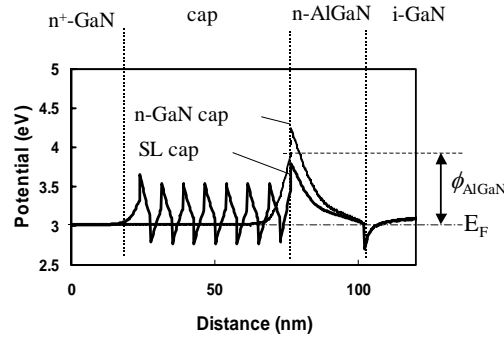


Fig. 2. Calculated conduction band profiles of an SL (solid line) and a GaN (dotted line) cap HFETs.

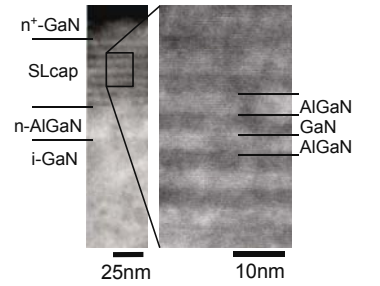


Fig.3 Transmission electron microscope images of an SL cap.

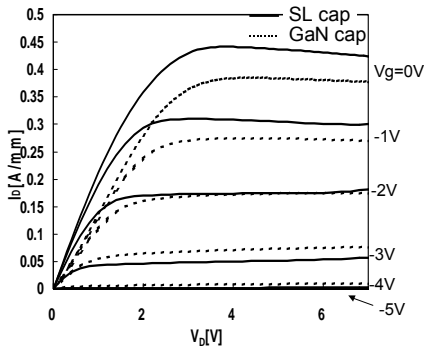


Fig.4 Drain characteristics of fabricated SL and GaN cap HFETs.

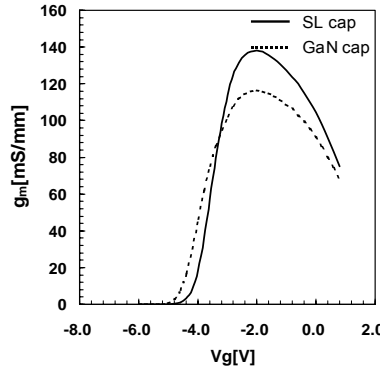


Fig.5 Transconductance vs. gate voltage characteristics of fabricated SL and GaN cap HFETs. The  $V_D$  was applied to 5V.

