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Nanoelectronic Scaling Tradeoffs: What does Materials Physics have to say?

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1. Introduction

In this paper, we discuss three "Grand Themes" of the future nanoelectronics: 1) Materials by Design, 2) Thermal Physics at the Nanoscale, 4) Nanodevices Beyond the End of Si CMOS scaling

2. Materials by Design

The idea of Materials by Design is to focus strengths in materials, characterization, and modeling to develop a foundational knowledge base and predictive modeling infrastructure for the design of materials exhibiting specified properties.

A Grand Challenge in Materials by Design is to develop the capability to predict and realize the existence of a material that satisfies a given set of specifications. "Existence Theorems" are needed for realizable materials that meet a behavioral specification. For example, gate insulator materials are needed that combine the property of high dielectric constant K with large band gap E_g. However, in the conventional dielectrics, the dielectric function is a decreasing function of the band gap. Is it possible to synthesize material with bandgap e.g. closest to the highest known in solid materials ($E_{g\ max}$=14 eV for LiF) and dielectric constant in the range of 80-100? This would provide a solution for the gate insulator for high-performance logic devices.

Another example for devices based on quantum mechanical tunneling, relates to the need to create build-in potential barriers of special profile. For example, graded (e.g. "crested") tunneling barrier shape has been shown to be useful for nonvolatile memory devices for nonvolatile memory devices [2, 3,]. To form a barrier of such a shape, a layered dielectric structure needs to be formed, where the bandgap E_g and the dielectric constant K differs from layer to layer. Such structures, in principle, could enable floating gate semiconductor memory with very fast write/erase operation in ns range and a very long retention time of many years [3]. The concept of a floating gate with engineered tunnel barrier is very attractive, however the realization of layered dielectric tunnel barrier is very difficult and has not yet experimentally demonstrated.

Indeed, the ability to make dielectric tunnel barriers of arbitrary shape could lead to new families of nanoelectronic devices that require new dielectric materials with graded E_g and K. A challenging goal for Materials by Design would be to systematically form graded structures from dielectric materials.

3. Thermal Physics at the Nanoscale

A critical challenge facing the semiconductor industry is to maintain the trend in power and performance efficiency of integrated circuits. The technology scaling, high operating frequencies, and dense packing of nanoelectronic components for information processing typically results in increased levels of dynamic and static power dissipation and therefore, heat. Heat removal is becoming more complex as we add new materials such as SOI, high K gate dielectrics, increased layers of interconnects and 3-D integration. Therefore, scaled charge-based electronics is likely to create very high power dissipation and heat generation. Indeed, the estimated levels of generated heat may exceed 1000 W/cm^2, which is approximately the capability limit of known heat removal systems.

One approach is to minimize energy consumption on the level of individual device, such as binary switch (e.g. FET). However, it appears unlikely that known alternative binary switches such as e.g. single electron, molecular, or carbon nanotube devices can operate at much lower energy in practical circuits, than CMOS devices. Moreover, even at the fundamental limit of k_BTln2 per bit operation for electron transport devices, heat generation theoretically could reach MW/cm^2 for dense arrays of switches a few nm in size operating at attainable switching speeds [4].

Another approach is to maximize the rate of heat removal. The key materials-related problem arises from the very nature of information processing and can be described as *the barrier dilemma*. Energy barriers are key components used to *information flow* in electronic information processing systems. Barriers are needed for charge transport to enable distinguishability of binary states [4]. These barriers are made of heterointerafces. However, interfaces impede the transport of phonons, since interfaces constitute interruption in the regular crystalline lattice on which phonons propagate [5]. For example, in the acoustic-mismatch model, the transmission coefficient T_{AB} for phonon energy incident normal to the interface with materials B is given by [5]:

$$T_{AB} = \frac{4Z_A Z_B}{(Z_A + Z_B)^2} \qquad (1)$$

where $Z=\rho c$, ρ is mass density and c is speed of sound.
In a semiconductor chip, there are billions of interfaces. As a result the heat removal rate from the heterogonous materials system is considerably lower than from a homogeneous solid, e.g., silicon.

In longer-term perspective a broad strategy must be implemented to address more generally the problem of

heat removal from terascale complex matter. New ideas are needed that enable heat removal at rates that are orders of magnitude greater than techniques known today. For example, the feasibility of ballistic methods for heat removal such as stimulated phonons/heat lasers, solitons, photon emission and photon engineering concepts may offer opportunities for improved thermal management technologies.

4. Emerging Research Memory and Logic Devices identified by 2003 ITRS

The 2003 International Technology Roadmap for Semiconductors (ITRS) provides assessments of alternative concepts for memory and logic devices that would, if successful, substantially extend the Roadmap beyond CMOS [1]. The emerging candidates for memory and logic devices are listed in tables I and II. A practical implementation of these emerging devices requires an extensive materials research.

Table I. Emerging Research Memory Devices

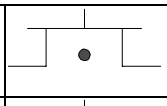
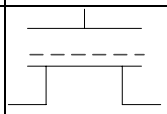
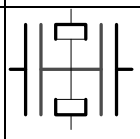
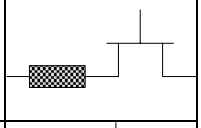
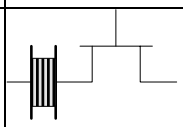
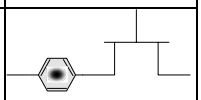
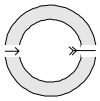
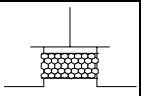
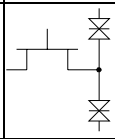
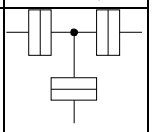
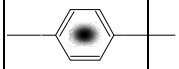
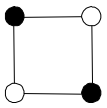
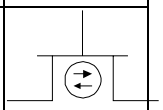
Device	**Operation Mechanism**	
I. Capacitive Memory Element		
Floating body DRAM	Charge stored in body of PDSOI MOSFET	
Nanofloating Gate Memory	FLASH with engineered tunnel barrier OR charge stored on silicon nano-crystals	
Single-electron memory	Charge stored on a quantum dot channel of an Single Electron Transistor	
II. Resistive Memory Element		
Phase-Change memory	R=*f*(crystalline- or amorphous- phase)	
Insulator resistance change Memory	R=*f*(formation or dissolution of metal nanowire)	
Molecular Memory	R=*f*(bias voltage)	

Table II. Emerging Research Logic Devices

Device	**Operation mechanism**	
Rapid Single Flux Quantum Devices (RSFQ)	Tunneling in superconducting structures	
1D structures	Drift electron transport in nanowires and nanotubes	
Resonant Tunneling Devices (RTD)	Resonant tunneling in semiconductor heterostructures	
Single Electron Transistors (SET)	Single electron tunneling and coulomb blockade	
Molecular devices	Electron transport in molecules	
Quantum Cellular Automata (QCA)	Tunneling	
Spin Transistors	Spin transport in transistor structure	

5. Conclusions

The semiconductor industry has established an aggressive goal to continue Moore's Law scaling for the next fifteen years, obtaining features sizes below 10 nanometers in the limit. There are fundamental materials science issues that should be resolved for a successful implementation of integrated nano-scale devices.

References

[1] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors*, 2003 edition, Austin, TX: International SEMATECH, 2003

[2] K. K. Likharev, IEEE Circ. Dev. **16** (2000) 16

[3] J. D. Casperson, L. D. Bell, H. A. Atwater, J. Appl. Phys. **92** (2002) 261

[4] V.V. Zhirnov, R. K. Cavin, J. A. Hutchby, G. I. Bourianoff, Proc. IEEE **91** (2003) 1934–1939

[5] D. G. Cahill, W. K. Ford, K. E. Goodson, G. D. Mahan, A. Majumdar, H. J. Maris, R. Merlin, S. R. Phillpot, J. Appl. Phys. **93** (2003) 793