Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 62-63

E-1-2

Dopant Profiling in Vertical Ultrathin Channel for Double-gate MOSFET by Scanning Nonlinear Dielectric Microscopy (SNDM)

M. Masahara, S. Hosokawa, T. Matsukawa, K. Endo, Y. Naitou, H. Tanoue and E. Suzuki
Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan, Tel: +81-29-861-3488, E-mail: m.masahara@aist.go.jp

1. Introduction

The double-gate MOSFETs (DGFETs), where an ultrathin channel (UTC) is sandwitched by two gates, have been widely recognized as the best candidates for the scaled CMOS [1]. Among them, vertical UTC DGFETs, e.g., FinFET [2] and vertical DGFET [3], have been attracted considerable attention due to their process simplicity (Fig. 1). So far a number of studies have experimentally proved their high performances. However, as the device size is scaled down, the source/drain (S/D) formation by an ion implantation (I/I) process becomes of big concern for the vertical UTC DGFET fabrication. This is due to the difficulty of the doping control in the UTC. Due to the vertical configuration of the channel, highly angled I/I is inevitable. This complicates the dopant profile in the UTC. Also, dopant diffusion in the UTC has not been clearly understood yet. SIMS analysis cannot be applied any longer to investigate the dopant profile in the vertical UTC.

In this work, to solve this problem, we have tried and succeeded in profiling the dopant in the vertical UTC for the vertical DGFET using a scanning nonlinear dielectric microscope (SNDM), a variation of a scanning capacitance microscope (SCM), for the first time. This paper demonstrates the nm-scale dopant profiling and quantitative measurement of the channel length in the vertical UTC for the DGFET by using SNDM.

2. Experimental

A vertical UTC was formed on a p-type (110) Si substrate. The height of UTC was 175 nm, and the thickness was varied from 18 nm to 58 nm. The doping concentration of the substrate was set at 2 x 10^{17} cm^{-3}. After the UTC formation, As ions were irradiated on the UTC (Fig. 2(a)). The angled I/I was employed to form an abrupt p-n junction in the top and bottom of the UTC. This I/I process corresponds to the S/D formation for the vertical DGFET [3]. After the TEOS deposition, the dopants were activated at 850^{o}C for 30 min (Fig. 2(b)). The samples were then cross-sectioned by cleaving and were beveled by polishing (Fig. 2(c)). The beveled angle was below 1^{o}, which results in amplifying the vertical size of the UTC by about 10^2. Finally the sample surfaces were prepared with the RCA cleaning and HF dipping and then covered with an oxide formed by low-temperature oxidation under UV irradiation at 300^{o}C, 40 min [4]. SNDM measurements were performed using an SPM unit (Seiko Instruments Inc., SPA-300HV) in a vacuum (~ 10^{-5} Pa) with a Rh-coated cantilever [5].

3. Results and discussion

Figure 3 shows the SEM image of the UTC before and after the beveling. Thanks to the beveling, *dC/dV* signal profiles of the top and bottom region of the UTC can be successfully obtained with nm-scale resolution as shown in Fig. 4 and 5. As shown in Fig. 4(b), the top region of the UTC shows a negative *dC/dV* signal, which means, the top region is n^+ type. Then the *dC/dV* signal is gradually lowered and reaches a minimum. This dip represents a reduction in the electron concentration at the edge of the n^+ region. The *dC/dV* signal next increases and reaches the zero point (indicated by an arrow in Fig. 4(b)). According to the commonly accepted scheme, this point is defined as the junction position [6]. After that, the *dC/dV* signal should increase to positive value due to p-type channel as surely confirmed in the profile for the bottom of the UTC case (Fig. 5(b)). However, for the top of the UTC case, the *dC/dV* signal keeps around zero as shown in Fig. 4(b). This phenomenon is commonly observed for all the UTC. We thus consider that this arises from the carrier depletion due to a thin and short channel. Although a positive *dC/dV* signal is not yielded from the p-type UTC, the dip profile which represents an edge of n^+ region is definitely observed for any UTC. So, for the UTC, we can define the junction position as the point where the *dC/dV* signal first reaches the zero after the dip according to the common scheme.

The dependence of the *dC/dV* profile in the top region of the UTC on the I/I energy is shown in Fig. 6. It is obvious that the junction position shifts downward as the ion energy and dose are increased, which means that the n^+/p junction depth becomes deeper.

Figure 7 shows the channel thickness (T_c) dependence of the *dC/dV* profile for the top of the UTC. It should be noteworthy that the junction position moves to an upper position with decreasing T_c. Especially, for the thinnest T_c case, the junction position significantly shifts upward. This clearly shows that a significant dopant loss occurs in the top region of the thinnest UTC. We speculate that this dopant loss originates in scattering out of As ions from the UTC during I/I and piling up of As ions at the surface during an activation [7].

For the vertical DG-MOSFET, we can define the channel length L_c as the length between the n^+/p junction at the top of the UTC and the bottom. We then estimated the L_c from the obtained *dC/dV* profiles quantitatively and compared with that predicted from SIMS analysis as shown in Fig. 8. In the SIMS analysis, we referred to a dopant profile in the bulk Si substrate in order to estimate the L_c. The L_c for the thicker UTC fairly agrees with that predicted from SIMS analysis. On the other hand, the L_c for the thinner T_c becomes longer probably due to a significant dopant loss. Accordingly, I/I condition should be carefully optimized for the S/D formation in the vertical UTC for the DGFET, e.g., a FinFET or a vertical DGFET.

4. Summary

Dopant profiling in the vertical UTC and quantitative estimation of the channel length for the vertical DGFET with nm-scale resolution were carried out using SNDM, for the first time. Thanks to a high resolution SNDM technique, it was found that the channel thickness significantly influences the ion doping into the UTC. The obtained results provide an important guideline for the S/D engineering in the scaled UTC DGFET.

Acknowledgements: This work was partly supported by NEDO.

References: [1] T. Sekigawa, et al., Solid-State Elec. 27(1984)827. [2] Y. Liu, et al., IEDM(2003)986. [3] M. Masahara, et al., IEDM(2002)949. [4] V. V. Zavyalov, et al., Rev. Sci. Instrum. 70 (1999)158. [5] T. Matsukawa, et al., APL(2004)3169. [6] J. J. Kopanski, et al., JVST-B16(1998)339. [7] M. Koh-Masahara, et al., JJAP,38(1999)2324.

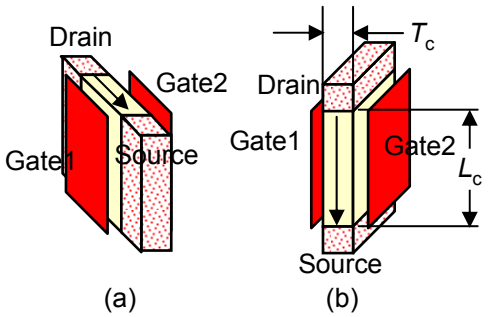

Fig. 1: Vertical UTC DGFETs. (a) FinFET, (b) Vertical DGFET. Arrows indicate current flow direction.

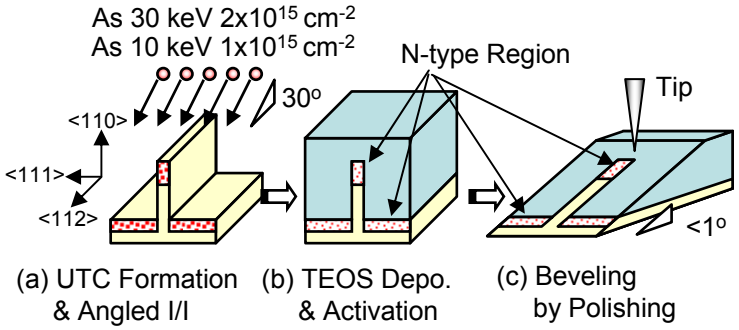

Fig. 2: Sample preparation process flow.

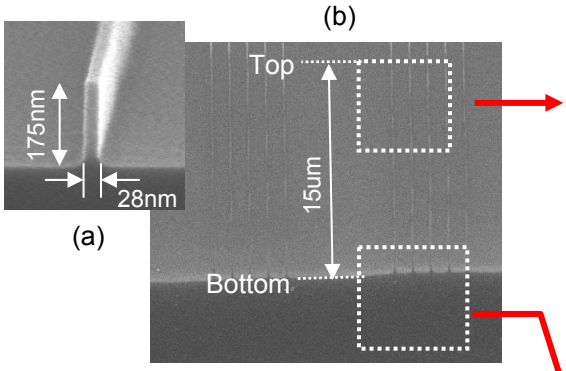

Fig. 3: (a) XSEM image of the 28-nm-thick UTC. (b) Top view of the multi-UTCs after beveling.

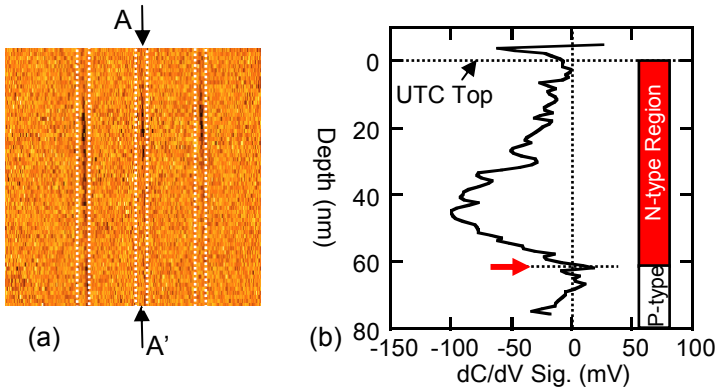

Fig. 4: (a) SNDM image of the top region of 28-nm-thick UTC and (b) X-profile of *dC/dV* signal across A-A'.

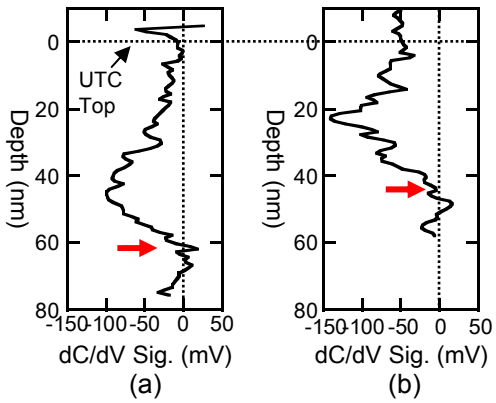

Fig. 6: I/I energy dependence of X-profile of *dC/dV* signal across n^+/p junction formed in the UTC top region. (a) As 30 keV, 2x10^{15} cm^{-2}, (b) As 10 keV, 1x10^{15} cm^{-2}. As the I/I energy and the dose increase, n-type region extends downward.

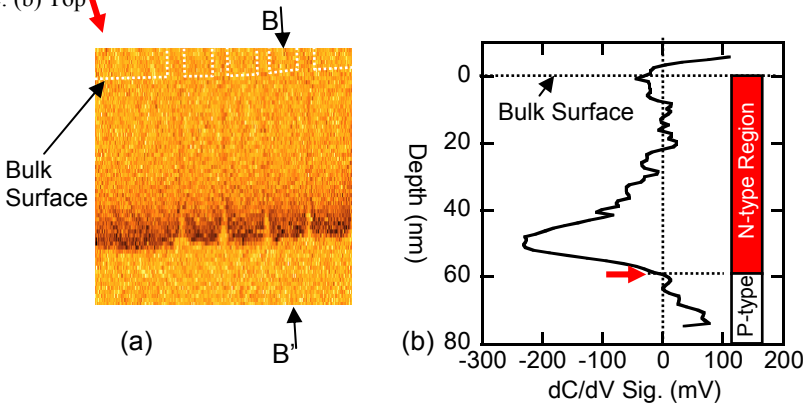

Fig. 5: (a) SNDM image of the bottom region of UTC and (b) X-profile of *dC/dV* signal across B-B'.

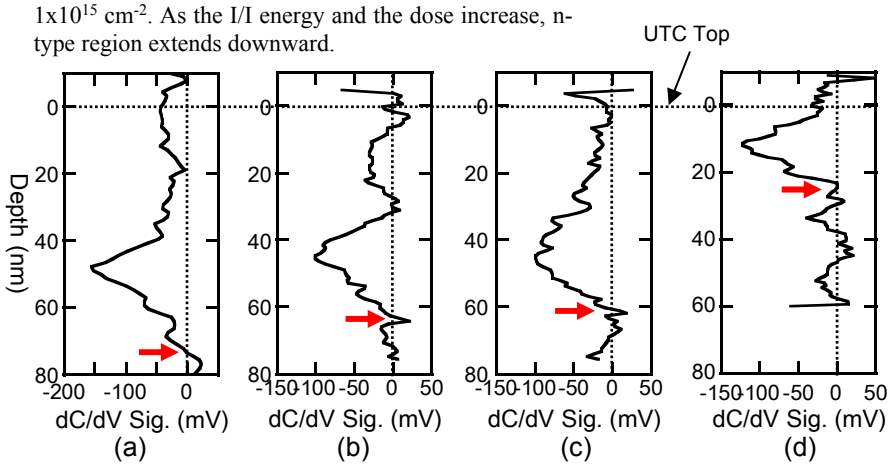

Fig. 7: Channel Thickness dependence of X-profile of *dC/dV* signal across n^+/p junction formed in the UTC top region. (a) T_c = 58 nm, (b) T_c = 38 nm, (c) T_c = 28 nm, (d) T_c = 18 nm. As T_c decreases, top n-type region shrinks.

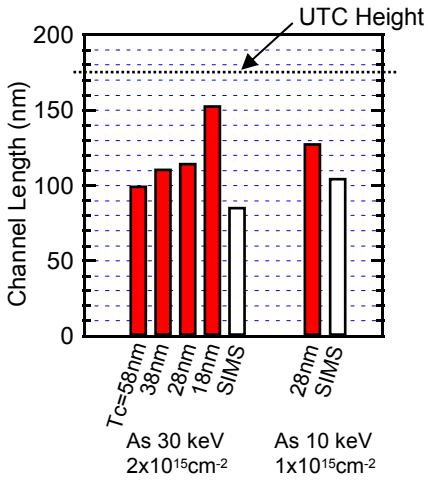

Fig. 8: Comparison between the L_{ch} obtained from *dC/dV* profiles and the metallurgical channel length (L_{met}) predicted from SIMS analysis.