Study of L_{GATE} dependence of 2-D carrier profile in N-FET by Scanning Tunneling Microscopy

Hidenobu Fukutome, Takayuki Aoyama and Hiroshi Arimoto¹

FUJITSU LABORATORIES LTD., Silicon technologies laboratories, Advanced CMOS technology lab. 50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan

Phone: +81-42-532-1250, Fax: +81-42-532-2513, E-mail: fukutome@jp.fujitsu.com

¹FUJITSU LTD., Advanced LSI development div.

50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan

1. Introduction

To obtain small and highly powerful devices, it is very important to optimize the design of two-dimensional (2-D) carrier profiles in the active regions, e.g. source/drain and extension (SDE) regions of metal oxide semiconductor field-effect transistors (FETs). It has been reported that we can measure such 2-D carrier profiles around SDE regions on a nanometer scale with the use of scanning tunneling microscopy (STM) [1, 2]. Actually, we have evaluated its dependence on fabrication processes to optimize electrical properties of FETs, for example, Vth roll-off characteristic [2-3]. We believe that the origin of such roll-off characteristics can be directly evaluated from STM images of FETs with various gate lengths (Lg). In this study, 2-D carrier profiles of n-FET with various Lg will be measured by STM. These profiles will be compared with the Vth roll-off characteristic of the corresponding device.

2. Experimental

N-FET samples for STM measurements were prepared under a standard fabrication process without source/drain implantation as shown in Figure 1. After H-terminated cross-sectional planes were prepared, 2-D carrier profiles were obtained by using STM [2]. We could evaluate carrier (potential) profiles in the channel regions, which were either partially or entirely depleted by the extension region, from tunneling currents (schematically shown in Fig. 1).

3. Results and discussion

Figure 2 shows the Vth roll-off characteristic of the n-FET. The threshold voltage monotonously decreased due to a "short channel effect". The geometric outline of the n-FETs including silicon recesses could be observed as the topographic STM images (Fig. 3). For simplification, the following STM current images (carrier profiles) are indicated with the schematic outline obtained from the topographic images. Figures 4(a)-4(c) show the 2-D carrier profiles of the n-FETs with Lg of 150 nm, 45 nm and 37 nm, respectively. The carrier profiles around channel and extension regions were visualized together with depletion layers. In the 150 nm n-FET, the abruptness of 3 nm/decade was almost the same between the vertical and lateral extension profiles (Fig. 5). However, the vertical depletion layer with the length of 69 nm was spread longer than the lateral one with the length of 44 nm (Fig. 6). This suggests

that the carrier concentration in the channel around the lateral extension edge was twice higher than that around the vertical extension edge. Then, The extension overlapping length of 10 nm did not depend on the Lg. In contrast, Lg-dependence of the lateral channel profile could be observed. The channel region was completely depleted when the Lg was shorter than 50 nm. When the Lg was 45 nm, the width of the depleted channel ($I_{\text{left}}\text{-}I_{\text{right}}$ distance in Fig. 7) was about 20 nm. This sufficient distance suppressed S/D leakage current without a strong negative gate voltage. When the Lg was 37 nm, the I_{left} - I_{right} distance was only 7 nm even though abruptness of the lateral potential profile became steeper due to relatively higher channel concentration (pocket impact from both side). The pocket impact on the extension region was more significant in the deeper region in the n-FET with the Lg of 37 nm (Fig. 8). The decrease of the extension overlapping at a depth of 20 nm was about 10 nm while that was only 4 nm in the n-FET with the Lg of 150 nm. The excess pocket impurities from the opposite side made the extension overlapping decrease and made the potential distribution in the deep channel gentler than that in the top channel. Based on such profiles, it was confirmed that some negative gate bias voltage was necessary for the top channel to realize the off state in the n-FET with the Lg less than 37 nm. Therefore, the dependence of the channel profile on the Lg was consistent with the Vth roll-off characteristic of the corresponding device.

4. Conclusions

We measured the 2-D carrier profiles of the n-FETs with the various Lgs using STM. In the n-FET with the Lg of 37 nm, the effect of the pocket impurities from the opposite side mainly appeared as the reduction of 6nm in the extension overlapping at a depth of 20 nm. Although such a pocket made the top channel concentration increase, the distance of the S/D tunneling path was 7 nm and was much shorter than that of 20 nm in the 45 nm n-FET. This insufficiency resulted in the negative Vth as shown in the Vth roll-off characteristic of the corresponding device.

References

- [1] H. Fukutome, et al., IEDM Tech. Digest, 67 (2001).
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Fig. 1 fabrication flow of STM samples and schematic illustration of relationship between tunneling current and carrier profile



Fig. 2 Vth roll-off characteristic of the n-FET



Fig. 3 Topographic STM image of the 50 nm n-FET



Fig. 4 2-D carrier profiles of the n-FETs (a) Lg=135nm, (b) Lg=45nm, (c) Lg=37nm.



Fig. 5 Comparison between the lateral and the vertical profile across the extension region of the 150 nm n-FET



Fig. 6 Comparison between the lateral and the vertical depletion layers spread in the 150 nm n-FET



Fig. 7 Lateral depleted channel profiles near the gate insulating layer in the n-FETs



Fig. 8 Relationship between the depth and lateral channel profiles of the n-FETs with the gate length of 38 nm