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Influences of Traps within HfSiON Bulk on Positive- and Negative-Bias Temperature Instability of HfSiON Gate Stacks

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1. Introduction

Hf-silicate is a promising high-k gate material [1]. However, it traps a high density of electrons, resulting in the positive-bias temperature instability (PBTI) [2, 3]. Nitridation seems to reduce the PBTI by making the Hf-silicate films amorphous [3, 4], but it may worsen the NBTI reliability [5]. To achieve the fabrication of a highly reliable gate stack, we investigated how PBTI and NBTI occur in the HfSiON gate. We show that electron trapping is involved in the NBTI as well as in the PBTI and that the subthreshold slope tends to be reduced by the BT stress. We attribute these BTI behaviors differing from those in SiON to the traps present within the HfSiON bulk.

2. Experimental

The poly-Si gate MOSFETs we examined typically had EOTs of 1.6-1.8 nm. The gate leakage current (in nMOSFETs) relative to that of SiO_2 gate was less than 10^{-2}. The typical threshold voltage (V_{th}) was +0.43 V (n) and -0.92 V (p). The carrier mobility relative to that of SiO_2 gate, obtained with the best process condition, was 0.96 (n) and 0.98 (p). We used MOSFETs with a channel length/width of 0.6/10 μm. Constant gate bias was applied to the FETs at temperatures from RT to 85°C. The V_{th} and subthreshold slope (*S*) were evaluated from the drain current measured at the stress temperature. Interface trap density (D_{it}) was evaluated from the charge-pumping (CP) current at RT. In order to suppress the recovery of the BT-stressed FETs, a low bias voltage of the same polarity as that of the stress bias was applied during the cooling.

3. Results and Discussions

Figure 1 shows the variation of ΔV_{th} with the fabrication processes. A stress bias that corresponded to an effective electric field ($[V-V_{th}]/EOT$) of ±0.8 V/nm was applied at RT for 100 s. The ΔV_{th} values in the PBTI were evidently large and strongly depended on the process conditions, when compared with those in the NBTI. The crystallized HfSiON (*c*-HfSiON: *B*, *E*, and *G*) had larger ΔV_{th} values of the PBTI, while the V_{th} of the amorphous HfSiON (*a*-HfSiON: *A*, *C*, *D*, and *F)* shifted little.

Besides the ΔV_{th} magnitude, *c*- and *a*-HfSiON showed a difference in the time dependence factor of the ΔV_{th} (n of t^n, at the initial stage of the PBTI) and a difference in the electron capture cross sections (σ), as shown in Fig. 2. The *n* was about 0.3 for *c*-HfSiON, while it was about 0.2 for *a*-HfSiON. And the σ at an effective electric field of 0.85 V/nm, estimated by extrapolating the data in Fig. 2, was 8×10^{-22} cm^2 for *c*-HfSiON, while it was much smaller (3×10^{-23} cm^2) for *a*-HfSiON. Thus, the kinetics of electron trapping seems to strongly depend on the structure of the HfSiON films.

Figure 3 shows representative data of ΔV_{th} against stress duration that were taken from another set of MOSFETs with *a*-HfSiON gates. The time dependence factor (n: $\Delta V_{th} \propto t^n$) was 0.20-0.22 for the PBTI and it was 0.17-0.20 for the NBTI. We estimated the ΔV_{th} values after 10 years at 85°C ($\Delta V_{th}(10y)$), by assuming that ΔV_{th} exponentially depends on the stress bias. The $\Delta V_{th}(10y)$ was 12 mV at +1.2 V for the PBTI and it was -8 mV at V_{th}-0.7 V for the NBTI. The reason why we used V_{th}-0.7 V instead of -1.2 V is that the $|V_{th}|$ of pMOSFETs was too high in the present samples, possibly due to a Fermi-level pinning at the interface of poly-Si and HfSiON [6]. Apart from the V_{th} issue, it was shown that the PBTI and NBTI could be suppressed to acceptable levels by using *a*-HfSiON.

Figure 3 also shows the ΔV_{th} dependence on the stress temperature. Differing from the previous report on a HfO_2 gate [2], the ΔV_{th} in the PBTI changed little with the temperature: The σ was almost constant up to 150°C. This may be because the trap species are not the same for HfO_2 and HfSiON. On the other hand, the ΔV_{th} in the NBTI was thermally activated. The activation energy (0.12 eV) was close to that of the NBTI in SiON gates. The NBTI of HfSiON gate may thus be due to the nitrogen incorporated at the HfSiON/Si interface.

Figure 4 shows the change of CP current by an application of a BT stress (ΔV_{th}= +13.9 or -15.6 mV). The CP current did not change in the PBTI, while it increased in the NBTI. This indicates that the PBTI occurs through electron trapping without generating interface traps, while the NBTI occurs through the generation of interface traps. Additionally, positive charges seem to be generated in the NBTI, since the density ratio of the interface traps to the net positive charges was less than unity ($[\Delta D_{it}E_g]/[C_{inv}\Delta V_{th}/q]$=0.47).

We compared (*a*) high N-content and (*b*) low N-content HfSiON gates that were made with a common process flow except for the nitridation. In Figs. 5 and 6, the ΔD_{it} and ΔS at 85°C are plotted against ΔV_{th}. The ΔV_{th} in the PBTI, normalized by the gate leakage current, was slightly higher for sample *b* (*b*/*a*=1.2). The ΔV_{th} in the NBTI, however, changed its polarity from the negative (*a*) to the positive (*b*). This indicates that electron trapping is also involved in the NBTI process. The ΔD_{it} in the NBTI was lower for sample *b* (*b*/*a*=0.6). This is presumably due to a suppression of the nitrogen-originated NBTI. We also note that the *S* tends to slightly decrease in the PBTI. Since the D_{it} remained almost constant in the PBTI, we attribute this negative ΔS to the electron traps within HfSiON: The spatial distribution of the trapped electrons may become uniform by the BT stress, which would decrease the subthreshold slope, like what seen in trap memory devices [7].

4. Conclusions

The PBTI of HfSiON gates was shown to be suppressed by using amorphous HfSiON, which we attribute to a reduction of the capture cross sections and the density of electron traps. The NBTI of HfSiON gates was found to involve electron trapping as well as the generation of interface traps and positive charges. Additionally, a decrease of the subthreshold slope was found to occur under the BT stress. These characteristic behaviors seem to be derived from the traps that are present within the HfSiON bulk.

References

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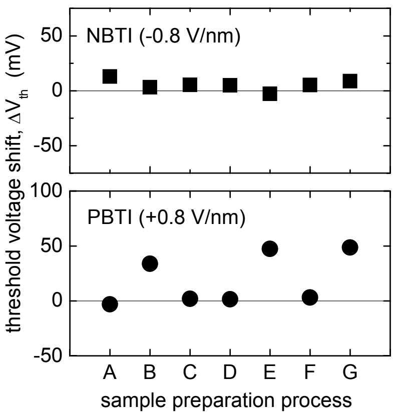

Fig. 1 Variation of V_{th}-shift with sample preparation processes. In the PBTI, *c*-HfSiON (*B*, *E*, and *G*) had large ΔV_{th}, while *a*-HfSiON (*A*, *C*, *D*, F) showed V_{th} shift little. In contrast, the NBTI did not depend much on the crystallinity of HfSiON.

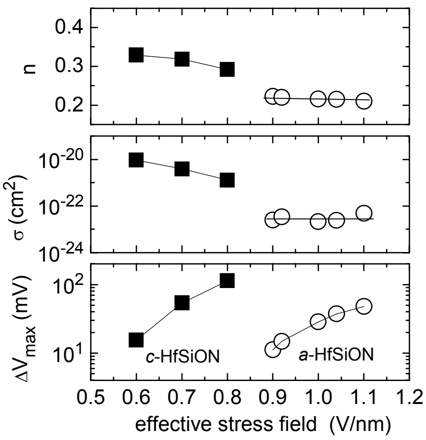

Fig. 2 Electron-trap parameters of *c*-HfSiON and *a*-HfSiON at 85°C evaluated by following Ref.2. ΔV_{th} data were fitted with an equation,
$\Delta V(t)=\Delta V_{max}\times\{1-\exp(-[Jgt/q\sigma]^{n})\}$.
The result indicates that the kinetics of the electron trapping changes with the crystallinity of HfSiON.

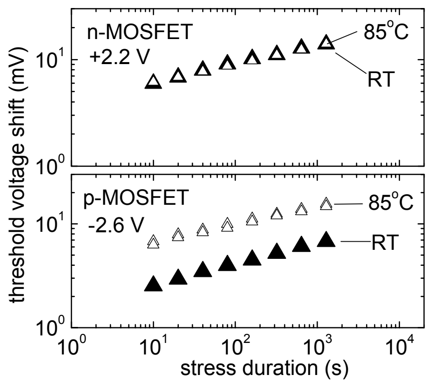

Fig. 3 V_{th} shift against stress durations at RT and 85°C. The time dependence factor (*n*) of the ΔV_{th} fitted by a function of t^{n} was 0.20-0.22 for the PBTI and it was 0.17-0.20 for the NBTI. It is also noted that the PBTI did not depend on the temperature, while the NBTI was thermally activated with an activation energy of 0.12 eV.

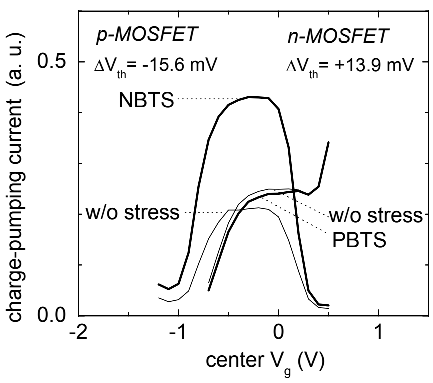

Fig. 4 Charge-pumping current at RT before and after an application of BT stress at 85°C. Interface trap density did not increase in the PBTI, while it increased in the NBTI. The increase of the signal of the n-MOSFET at Vg>0.4 V is due to the gate leakage current, not due to the charge-pumping current.

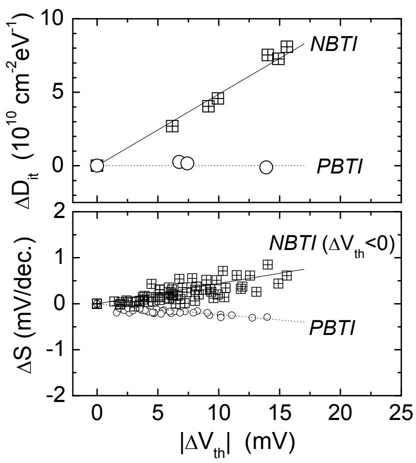

Fig. 5 ΔD_{it} and ΔS against ΔV_{th} of a *high* N-content HfSiON gate. In the PBTI, the D_{it} remained constant but the S slightly decreased. In the NBTI, the ΔV_{th} was *negative* and the D_{it} and *S* increased like those of SiON gates.

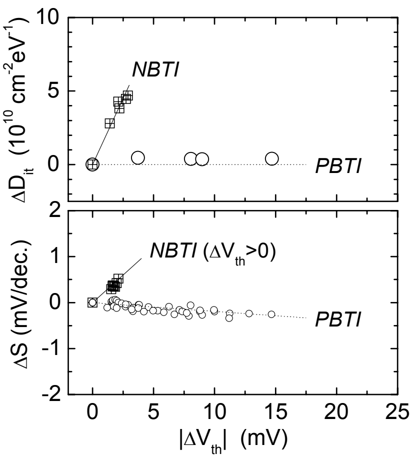

Fig. 6 ΔD_{it} and ΔS against ΔV_{th} of a *low* N-content HfSiON gate. In the PBTI, the D_{it} remained constant but the *S* slightly decreased. In the NBTI, the ΔV_{th} was *positive* unlike that of SiON gates, while the D_{it} and *S* increased.