Influences of Traps within HfSiON Bulk on Positive- and Negative-Bias Temperature Instability of HfSiON Gate Stacks

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1. Introduction
Hf-silicate is a promising high-k gate material [1]. However, it traps a high density of electrons, resulting in the positive-bias temperature instability (PBTI) [2, 3]. Nitrification seems to reduce the PBTI by making the Hf-silicate films amorphous [3, 4], but it may worsen the NBTI reliability [5]. To achieve the fabrication of a highly reliable gate stack, we investigated how PBTI and NBTI occur in the HfSiON gate. We show that electron trapping is involved in the NBTI as well as in the PBTI and that the subthreshold slope tends to be reduced by the BT stress. We attribute these BTI behaviors differing from those in SiON to the traps present within the HfSiON bulk.

2. Experimental
The poly-Si gate MOSFETs we examined typically had EOTs of 1.6-1.8 nm. The gate leakage current (in nMOSFETs) relative to that of SiO2 gate was less than 10^-2. The typical threshold voltage (Vth) was +0.43 V (n) and -0.92 V (p). The carrier mobility relative to that of SiO2 gate, obtained with the best process condition, was 0.96 (n) and 0.98 (p). We used MOSFETs with a channel length/width of 0.6/10 μm. Constant gate bias was applied to the FETs at temperatures from RT to 85°C. The Vth and subthreshold slope (S) were evaluated from the drain current measured at the stress temperature. Interface trap density (Dit) was evaluated from the charge-pumping (CP) current at RT. In order to suppress the recovery of the BT-stressed FETs, a low bias voltage of the same polarity as that of the stress bias was applied during the cooling.

3. Results and Discussions
Figure 1 shows the variation of ∆Vth in the fabrication processes. A stress bias that corresponded to an effective electric field ((V-Vth)/EOT) of ±0.8 V/nm was applied at RT for 100 s. The ∆Vth values in the PBTI were evidently large and strongly depended on the process conditions, when compared with those in the NBTI. The crystalized HfSiON (c-HfSiON: B, E, and G) had larger ∆Vth values of the PBTI, while the Vth of the amorphous HfSiON (α-HfSiON: A, C, D, and F) shifted little.

Besides the ∆Vth magnitude, c- and α-HfSiON showed a difference in the time dependence factor of the ∆Vth (η of τp, at the initial stage of the PBTI) and a difference in the electron capture cross sections (σ), as shown in Fig. 2. The η was about 0.3 for c-HfSiON, while it was about 0.2 for α-HfSiON. And the σ at an effective electric field of 0.85 V/nm, estimated by extrapolating the data in Fig. 2, was 8×10^-22 cm^2 for c-HfSiON, while it was much smaller (3×10^-23 cm^2) for α-HfSiON. Thus, the kinetics of electron trapping seems to strongly depend on the structure of the HfSiON films.

Figure 3 shows representative data of ∆Vth against stress duration that were taken from another set of MOSFETs with α-HfSiON gates. The time dependence factor (n: ∆Vth ∝ τp) was 0.20-0.22 for the PBTI and it was 0.17-0.20 for the NBTI. We estimated the ∆Vth values after 10 years at 85°C (ΔVth(10y)), by assuming that ∆Vth exponentially depends on the stress bias. The ΔVth(10y) was 12 mV at +1.2 V for the PBTI and it was -8 mV at Vth-0.7 V for the NBTI. The reason why we used Vth-0.7 V instead of +1.2 V is that the [Vth] of pMOSFETs was too high in the present samples, possibly due to a Fermi-level pinning at the interface of poly-Si and HfSiON [6]. Apart from the Vth issue, it was shown that the PBTI and NBTI could be suppressed to acceptable levels by using α-HfSiON.

Figure 4 shows the change of CP current by an application of a BT stress (ΔVth= +13.9 or -15.6 mV). The CP current did not change in the PBTI, while it increased in the NBTI. This indicates that the PBTI occurs through electron trapping without generating interface traps, while the NBTI occurs through the generation of interface traps. Additionally, positive charges seem to be generated in the NBTI, since the density ratio of the interface traps to the net positive charges was less than unity ([ΔD trap]/|CoxΔVth|/|CoxΔVth|/Q]≈0.47).

We compared (a) high N-content and (b) low N-content HfSiON gate that were made with a common process flow except for the nitridation. In Figs. 5 and 6, the ∆D and ∆S at 85°C are plotted against ∆Vth. The ∆D in the PBTI, normalized by the gate leakage current, was slightly higher for sample b (b/a=1.2). The ∆Vth in the NBTI, however, changed its polarity from the negative (a) to the positive (b). This indicates that electron trapping is also involved in the NBTI process. The ∆D in the NBTI was lower for sample b (b/a=0.6). This is presumably due to a suppression of the
nitrogen-originated NBTI. We also note that the $S$ tends to slightly decrease in the PBTI. Since the $D_n$ remained almost constant in the PBTI, we attribute this negative $S$ to the electron traps within HfSiON. The spatial distribution of the trapped electrons may become uniform by the BT stress, which would decrease the subthreshold slope, like what seen in trap memory devices [7].

4. Conclusions
The PBTI of HfSiON gates was shown to be suppressed by using amorphous HfSiON, which we attribute to a reduction of the capture cross sections and the density of electron traps. The NBTI of HfSiON gates was found to involve electron trapping as well as the generation of electron traps. The NBTI of HfSiON gates was found to decrease of the subthreshold slope was found to occur under the BT stress. These characteristic behaviors seem to be derived from the traps that are present within the HfSiON bulk.

References