Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 74-75

E-2-3

Breakdown Mechanisms and Lifetime Prediction for 90nm-node Low-power HfSiON/SiO_2 CMOSFETs

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Abstract

The gate leakage current and the TDDB failure mechanisms of HfSiON/SiO_2 gate dielectrics were investigated. The mechanisms are different under conditions of low or high electric field, due to the band height difference between interfacial SiO_2 and HfSiON. It was revealed that low-gate-bias FET measurement is necessary for precise TDDB lifetime estimation. A system that can detect defect generation by using an emission microscope was developed, enabling low-bias TDDB measurement of large gate area transistor for precise lifetime estimation. Through this investigation, it was experimentally confirmed that 90-nm-node HfSiON/SiO_2 CMOSFETs have sufficient reliability for practical usage (TDDB lifetime: 10^4 years at 85°C and 1.1 V).

1. Introduction

It is highly desirable to integrate high-k gate dielectric materials into CMOSFETs in order to reduce the device power usage [1-2]. Many investigation results such as mobility improvement [3-4], V_T control [2], and reliability improvement [5-8] have been reported. In this work, we investigated the gate leakage current and the TDDB failure mechanism for a gate insulator consisting of high-quality HfSiON/SiO_2 (EOT = 1.6 nm) for 90-nm low-power CMOSFETs.

2. Experiment

A synopsis of the process flow for HfSiON CMOSFETs with dual poly-Si gate electrodes is shown in Table I. In this investigation, we also fabricated MISFETs with a SiO_2 gate insulator for the reference. The electrical characteristics of the HfSiON/SiO_2 CMOSFETs fabricated for this study are indicated in Table II. A high mobility (N/PFET: 96/98%) and a lower leakage current (by a factor of 1/1000) as compared to SiO_2 were obtained. The N/PBTI characteristics were less than 4% of the I_{on} shift after 10 years of ±1.1 V stress at 85°C.

3. Results and Discussion

3-1. Gate Leakage Current Mechanisms:

Figure 1 shows the NMOS and PMOS inversion gate leakage current (I_G) with respect to the gate bias (V_G) for SiO_2 and HfSiON/SiO_2 gate insulators (EOT: 1.6 nm). In the NMOS case, at low voltage (1.0 V), the HfSiON FET exhibited I_G three orders lower than that of the SiO_2 FET. At higher voltage (3.0 V), the HfSiON I_G was less than one order lower as compared to that for SiO_2. On the other hand, the PMOS I_G was four orders lower for HfSiON independent of the gate bias.

Figure 2 shows simulation results for the NMOS inversion leakage current and the corresponding band diagrams. The NMOS leakage current behavior shown in Fig. 1 is well explained by these results. At lower voltage, electrons passed through both SiO_2 and HfSiON. At higher voltage, electrons passed through the interfacial SiO_2 band gap, however electrons pass above the conduction band edge of HfSiON. This is the reason for the increase in the NMOS I_G current at high voltage. Figure 3 shows (a) simulation results for the PMOS inversion leakage current and (b) actual carrier separation measurement results. Though the simulation results indicate that the main component of the PMOS gate leakage was holes, the measurements indicate a large electron current. It was considered that the electrons were generated by Fermi pinning at the gate electrode/HfSiON interface on the actual HfSiON FET. The large reduction in the PMOS inversion leakage independent of the gate bias magnitude, as seen in Fig. 1, can be explained that both electrons and holes passed through the HfSiON/SiO_2 layers.

3-2. TDDB Failure Mechanisms:

Figure 4 shows a TDDB Arrhenius plot for both negative and positive bias stress in N/PFETs. For NMOS inversion and PMOS accumulation, plots for different electric fields are also shown.

We first discuss the ***NMOS inversion*** breakdown mechanism. The activation energy (E_a:0.45 eV) of Q_{BD} under a high-bias condition, in which electrons from the substrate passed through only the SiO_2 layer, was the same as the E_a of reference SiO_2 (0.45 eV). This indicates that the lifetime was limited by interfacial SiO_2 breakdown. Under a low-bias condition, in which electrons from the substrate passed through the entire HfSiON/SiO_2 structure, E_a increased to 0.88 eV. The magnitude of the E_a increase due to electric field reduction was much greater than in the case of SiO_2 [9]. This indicates the change in lifetime limitation from interfacial SiO_2 to HfSiON. The large density of defect precursors with high activation energies in HfSiON caused it to break down.

Under the ***NMOS accumulation*** condition, in which electrons from the gate electrode passed through both the HfSiON and the SiO_2, the E_a (0.85 eV) for NMOS accumulation was very close to that for low-bias NMOS inversion. Figure 5 shows the NMOS Q_{BD} under the accumulation condition for three different HfSiON/SiO_2 films (A: 2.0 nm/2.0 nm, B: 3.0 nm/2.0 nm, and C: 3.0 nm/1.0 nm). A similar Q_{BD} value was observed with the same HfSiON thickness, independent of the base SiO_2 thickness. These results indicate that the HfSiON/SiO_2 lifetime was limited by HfSiON breakdown.

Under the ***PMOS inversion*** condition, in which electrons from the gate electrode passed through the entire HfSiON/SiO_2 structure, the E_a (0.82 eV) was very close to that for NMOS accumulation (Fig. 4). This indicates that the lifetime was limited by HfSiON breakdown in this case as well.

Next, we discuss the ***PMOS accumulation*** breakdown mechanism. The E_a (0.50 eV) under a high-bias condition, in which electrons passed through the SiO_2 layers, was similar to the NMOS E_a under highly biased inversion. It is considered that the lifetime was limited by interfacial SiO_2 breakdown. On the other hand, the E_a (0.87 eV) under a low-bias condition, in which electrons from the substrate passed through the HfSiON/SiO_2 layers, was high compared to that under the high-bias condition. This indicates that the lifetime was limited by HfSiON breakdown, just as in the case of low-bias NMOS inversion.

3-3.TDDB Lifetime Prediction:

Because of the stress bias polarity dependence on breakdown mechanism, accumulation stress measurement with MOS capacitor is not suitable for actual device lifetime estimation. In addition, electric field dependence indicated that HfSiON/SiO_2 lifetime estimation should be measured at low electric field. To investigate the actual breakdown time under a condition of low electric field, acceleration measurement with large gate area of MISFETs was necessary. Figure 6 shows the leakage current status during normal TDDB measurements, which detect increases in the leakage current as a means of soft breakdown detection. The breakdown leakage current increase caused by soft breakdown became negligible with increasing gate area. To determine the lifetime of large-gate MISFETs, we constructed a TDDB measurement system using an emission microscope, which can obtain breakdown images, as illustrated in Fig. 7. This system has sufficient resolution even for the soft breakdown detection. Figure 8 shows a summary of lifetime measurement results for fabricated CMOSFETs with HfSiON/SiO_2 and SiO_2 gate insulator structures. The HfSiON PMOS case exhibited a lifetime three orders greater (10^5 years) than that for SiO_2 at 1.1 V and 85°C. The HfSiON NMOS lifetime prediction line had a change of slope at about 2.6 V. These data confirm that an NMOSFET would also have sufficient lifetime for typical operation (10^4 years).

4. Conclusion

We have demonstrated the gate leakage current and breakdown mechanisms for HfSiON/SiO_2 CMOSFETs. Experimental results obtained with a TDDB measurement system using an emission microscope showed that CMOSFETs with this gate insulator structure would have a TDDB lifetime of more than 10 years at 85°C and 1.1 V.

References

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Table I. CMOS process flow

(1)Base Oxide Formation
(2)MOCVD-HfSiON Film Formation
(3)Poly-Si Deposition
(4)1050°C spike RTA

Table II. CMOS characteristics

EOT	1.6nm
Mobility	NMOS:96% PMOS:98%
I_G	NMOS:5.8E-4A/cm^2 PMOS:1.8E-5A/cm^2
Reliability (BT Instability) (@10years,85°C,±1.1V) NMOS PBTI <10mV PMOS NBTI <5mV	

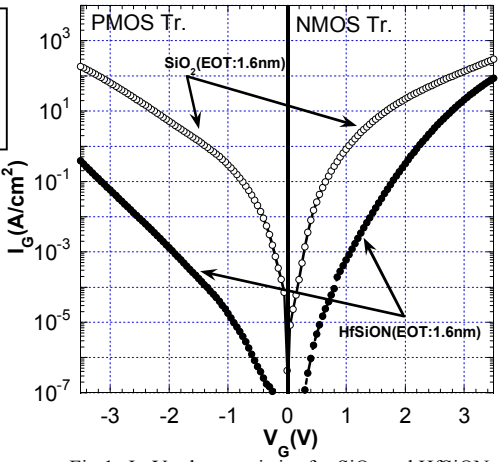

Fig.1 I_G-V_G characteristics for SiO_2 and HfSiON.

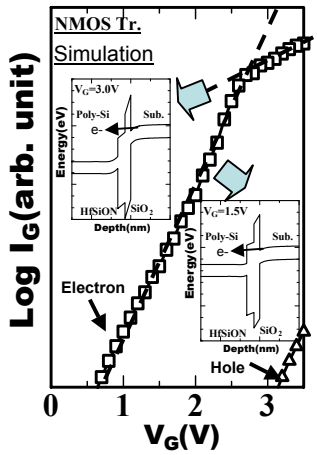

Fig.2 Simulation results for the NMOS inversion leakage current with the corresponding band diagrams.

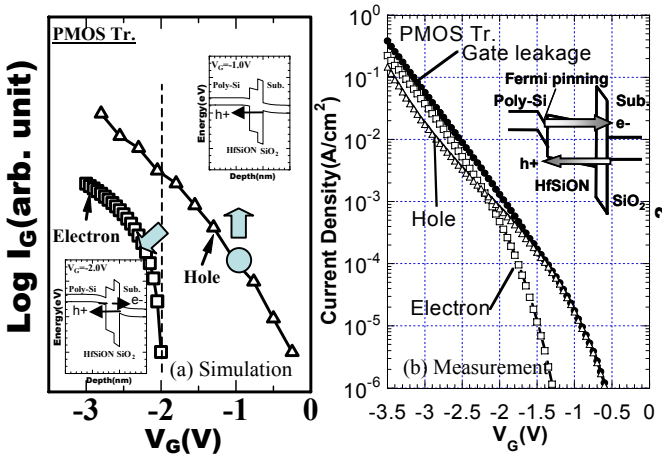

Fig.3 (a) Simulation results for the PMOS inversion leakage current with the corresponding band diagrams, (b) charge separation measurement results for the PMOS leakage current

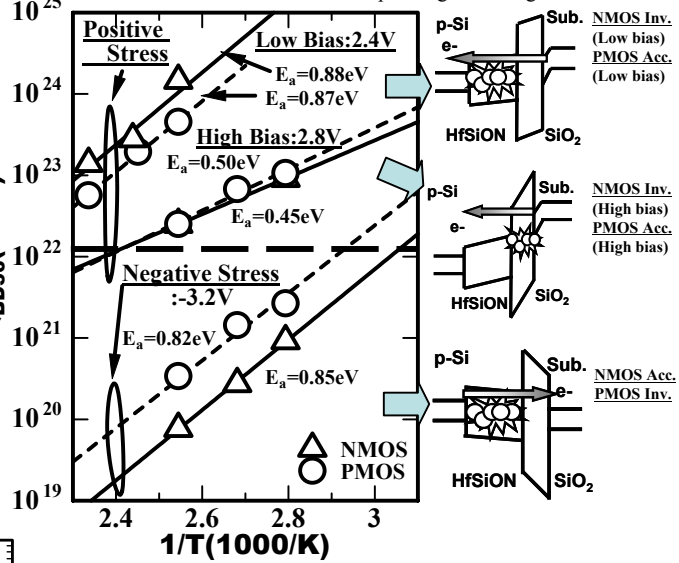

Fig.4 Arrhenius plots of the Q_{BD} (total charge through the insulator before breakdown) for both NMOS and PMOS FETs. The activation energies (E_a) and breakdown mechanisms are also shown.

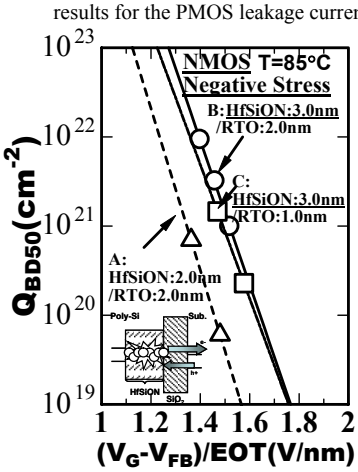

Fig.5 NMOS accumulation stress $Q_{BD(50\%)}$ for three types of FETs with HfSiON/SiO_2 layers as follows: A: 2.0nm/2.0nm, B3.0nm/2.0nm, C:3.0nm/1.0nm.

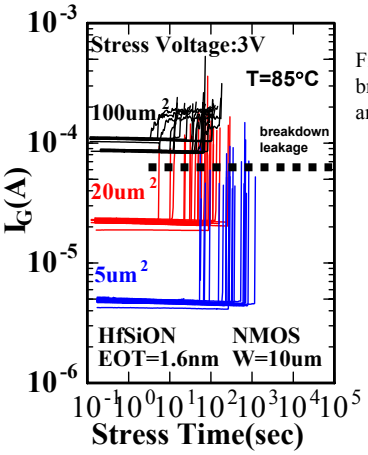

Fig.6 Area dependence of the NMOS TDDB characteristics. The breakdown level is also indicated.

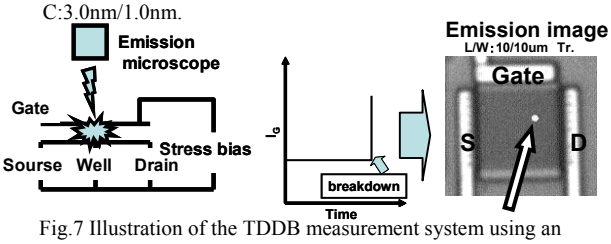

Fig.7 Illustration of the TDDB measurement system using an emission microscope.

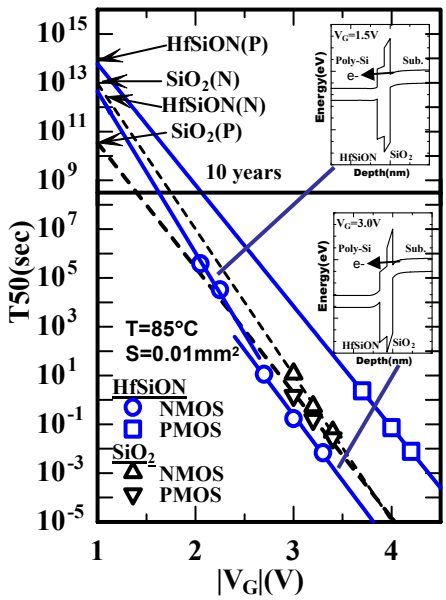

Fig.8 Lifetime prediction for HfSiON/SiO_2 and SiO_2.