Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 76-77

E-2-4

Degradation Mechanism of $HfAlO_X/SiO_2$ Stacked Gate Dielectric Films through Transient and Steady State Leakage Current Analysis

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1. Introduction

Since the first indication of the importance of high-k gate dielectrics, many efforts have been performed to understand various characteristics of those films. Much deeper analysis is still required to realize MOSFET with high-k stacks, for example, on the reliability model. As for the most realistic candidate for EOT = 1 nm high-k gate stack, we have already proposed $HfAlO_X$ structures fabricated by the *Layer-by-Layer Deposition and Annealing* (LL-D&A) process[1]. This paper proposes a degradation mechanism of $HfAlO_X/SiO_2$ stacks through the analysis of transient and steady state leakage currents.

2. Experimental

MOS capacitors and FETs with $HfAlO_X/SiO_2$ stacked dielectrics having various thickness combinations were fabricated on p- and n-type (100)Si. Thickness of each layer was evaluated by TEM. The measurements with capacitors were performed under the accumulation at the constant-voltage stress (CVS). N^+ gate p-ch MOSFETs were also measured for the carrier separation experiment[2].

3. Results and Discussions

Low Voltage Peak Current (LVPC) and SILC

Fig.1 shows initial I-V characteristics of $HfAlO_X/SiO_2$ stacked gate dielectrics having three $HfAlO_X$ thicknesses with fixed SiO_2 thickness of 1.3 nm. A leakage current peaked at ~ -0.5 V is observed. This leakage current is known in SiO_2 to be separated into the transient charging and the steady intrinsic currents[3]. Hereafter, this is referred to as the *low voltage peak current* (LVPC). The LVPC is not a local current because it is proportional to the gate area (not shown) and, hence, one cannot observe in small area samples. Fig.2 shows the $HfAlO_X$ (or SiO_2) thickness dependence of (a) peak voltage (V_P) and (b) peak current (I_P) of LVPC with fixed SiO_2 (or $HfAlO_X$) thickness. Despite of little impact of $HfAlO_X$ thickness, SiO_2 thickness strongly affects to both values. This indicates that the SiO_2 interlayer controls the conduction of LVPC.

Fig.3 shows the change in the I-V characteristics by cyclically performed CVS ($HfAlO_X/SiO_2$=8.6/1.3 nm). Both SILC and LVPC, defined as the gate current at -4 V and V_P, monotonically increase with stress time. Furthermore, V_P moves to the higher voltage, which may be the result of electron accumulation in $HfAlO_X$, and saturates finally as shown in the inset. Although saturated V_P depends on the stress voltage, we focus only on I_P in this paper. Time evolution of I_P under the application of V_P after each stress cycle was also measured as shown in Fig.4. I_P is proportional to the reciprocal of t (voltage application period) and, hence, LVPC has transient component such as charge trapping/detrapping processes.

Because LVPC is controlled by SiO_2, charge trapping/detrapping into/from $HfAlO_X$ through SiO_2, *i.e.*, (i) hole trapping and (ii) electron detrapping, are considered. Fig.5 shows the hole and electron (I_{hole}, $I_{electron}$) currents measured by the carrier-separation experiment using pMOSFETs. Significant I_{hole} with peaked shape is observed, while $I_{electron}$ is small. Thus, it is concluded that the hole trapping into $HfAlO_X$ through SiO_2 is the dominant mechanism of LVPC as illustrated in Fig.2. In Fig.2(a), Simulated SiO_2 thickness dependence of I_P with the presumption of tunneling through SiO_2 is plotted by a solid line. Simulation well reproduces the experiments and, therefore, above model is supported. Because of the $HfAlO_X$ thickness independence of I_P, hole trap sites exist mainly in the vicinity of $HfAlO_X/SiO_2$ interface. Here, it must be noted the electron detrapping from high-k layer through SiO_2 is the mechanism attributed to the origin of V_T instability[4]. On the other hand, existence of non-negligible amount of hole traps even without any electrical stress has been reveled. Considering the gate voltage region where the LVPC appears, the hole traps must be taken into account in the mechanism of V_T instability.

Degradation Mechanism

For the quantitative analysis, the time evolution of I_P under the application of V_P were fitted to the following equation and parameters I_0 and a were obtained:

$$I_P = I_0 + I_t = I_0 + a / t \qquad (1),$$

where I_0 and I_t are the steady state and transient state components and a is known to be proportional to the trap density mediating the transient component[3]. Fig.6 shows the behaviors of I_0 and a under -6.5 V CVS calculated from Fig.4. Abrupt increase in I_0 after ~20 s suggests the dominant current component change from transient to steady state. On the other hand, a keeps its rate throughout this stress time range. Fig.7 shows the behavior of the stress gate current (I_G), SILC, and the LVPC (I_P) under the -5 V CVS. Open squares show the transient component (I_t) calculated from a values. Again, transient component keeps its rate as indicated by broken line. This implies that the trap generation rate does not change throughout the stress, but the dominant conduction mechanism changes reflecting the sufficient generation of traps. This explanation can be also adopted to the gate current during CVS and SILC that show similar behaviors as shown in Fig.7.

Next, the relationship between LVPC and SILC is discussed. SILC is generally used as an measure of degradation[5][6] and, furthermore, dielectric breakdown[7]. The trap generation rate was obtained from a values of LVPC in the same way obtaining from SILC and was compared to that from SILC in Fig.8. A clear linear-relationship between both rates is obtained, implying the contribution of hole traps to the breakdown mechanism.

Finally, the degradation mechanism is proposed. Even in the unstressed condition, high-k gate stacks have

non-negligible amount of hole trap sites in the vicinity of high-k/SiO_2 interface. By the electrical stress, the density of hole trap site increases monotonically. It is expected that neutral trap sites that mediate the SILC are also generated having the correlation with the hole trap site generation. Considering the importance of the SILC as a measure of the integrity of dielectrics, the above findings will be useful also in the lifetime prediction of high-k gate stacks.

Acknowledgment

This work was supported by NEDO.

References

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4. Conclusion

In $HfAlO_X/SiO_2$ gate stacks, the *low voltage peak current* (LVPC) is observed even in the initial condition. The LVPC is controlled by the hole trapping into the trap sites near the $HfAlO_X/SiO_2$ interface through SiO_2 interlayer. By the electrical stress, hole trap sites monotonically increases having the correlation with SILC regardless of the dominant conduction mechanism change.

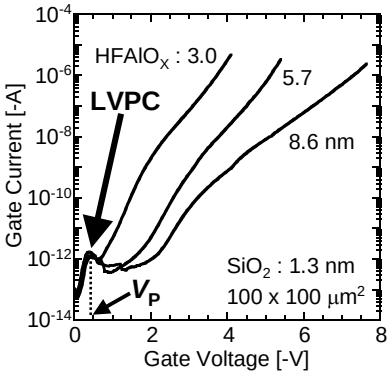

Fig.1 Initial current-voltage (I-V) characteristics of $HfAlO_X/SiO_2$ stacked gate dielectrics for three $HfAlO_X$ thicknesses with 1.3 nm interlayer SiO_2. The low voltage peak current (LVPC) at ~ -0.5V can be observed.

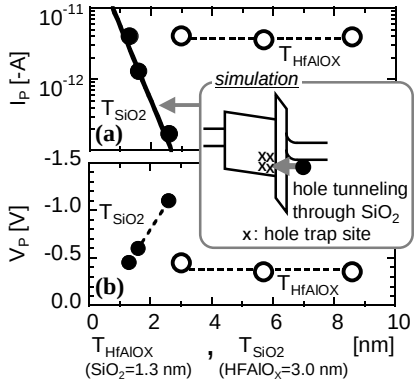

Fig.2 $HfAlO_X$ (or SiO_2) Thickness dependences of (a) peak voltage (V_P) and (b) peak current (I_P) of LVPC with fixed SiO_2 (or $HfAlO_X$) thickness. Solid line for I_P shows the simulated SiO_2 thickness dependence on the basis of proposed model.

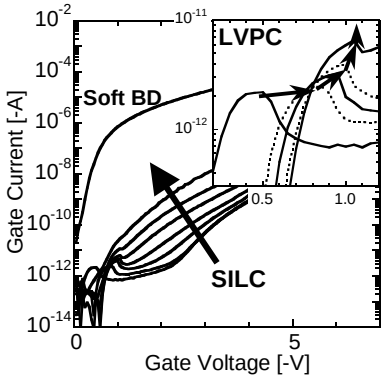

Fig.3 Typical change in I-V characteristics by cyclically performed -5.5 V constant-voltage stress (CVS). SILC and LVPC are defined as the currents at -4 V and at V_P, respectively. V_P moves to the higher voltage by stress and saturates finally.

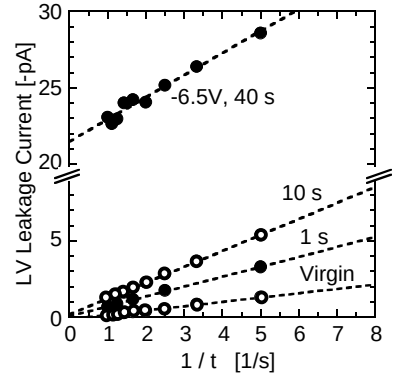

Fig.4 Time evolution of I_P under the application of peak gate voltage I_P (t: gate voltage application period) for samples unstressed (virgin) and stressed for various times from 1 to 40 s at -6.5 V. I_P is plotted as a function of 1/t.

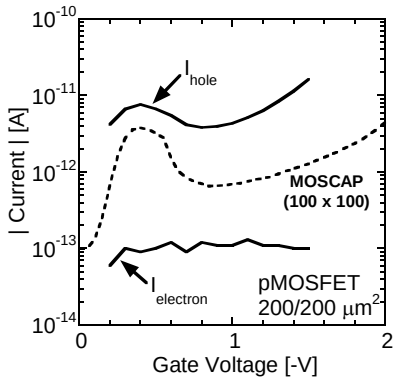

Fig.5 Hole (I_{hole}) and electron ($I_{electron}$) currents measured by the carrier separation technique with n^+ gate p-ch MOSFET ($HfAlO_X/SiO_2$ = 5.7/1.3 nm). Broken curve shows the I-V characteristics measured with an MOS capacitor with the same gate stack.

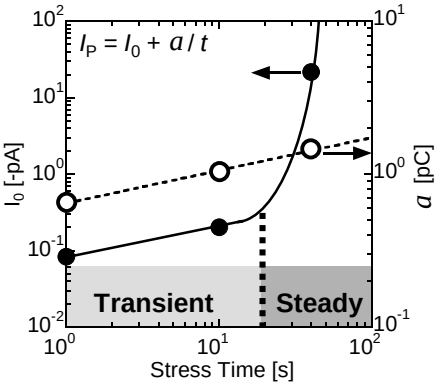

Fig.6 Behaviors of two parameters I_0 and a in Eq.(1) under -6.5 V CVS as function of stress time.

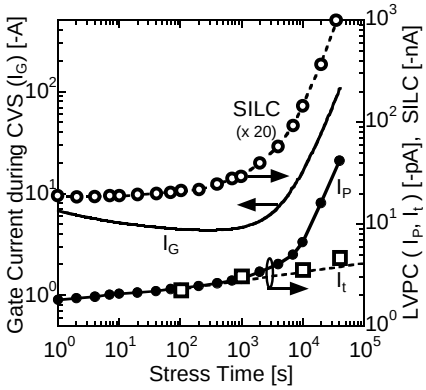

Fig.7 Behaviors of the gate current (I_G), SILC and LVPC (peak current: I_P , transient component: I_t) under -5 V CVS.

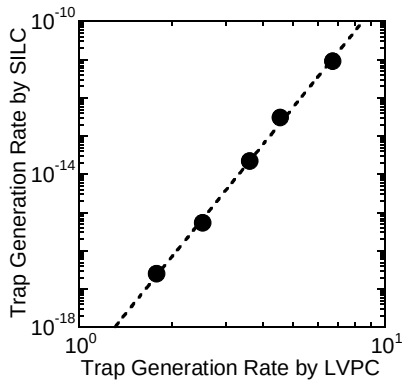

Fig.8 Relationship between the trap generation rate calculated from the SILC and that from the LVPC.