# Low Temperature Solution Processed SiO<sub>2</sub> Insulator Thin Films for Organic FET

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## 1. Introduction

Research on organic field effect transistor (OFET) is rapidly progressive over the past few years because of their possibility to applications in low cost and large area electronic devices prepared by low temperature solution process. Recently, in order to take such advantage of OFET, approach into the use of the gate insulator prepared by low temperature solution process has been performed by using polymeric dielectric materials such as polyimide [1], polyvinyl phenol [2], polyvinyl alcohol [3]. On the other hand, though it was well known that the thermal oxidation thin film of silicon dioxide (SiO<sub>2</sub>) was clearly superior for the gate insulator, it was difficult to prepare by low temperature solution process.

In this work, silazane compound was used as a precursor material for preparing a  $SiO_2$  thin film by solution process. The electronic property of insulator thin film and OFET were investigated.

## 2. Experimentals

Highly n-doped silicon wafers, whose resistivity was 1-10  $\Omega$ cm, was used as a substrate and electrode. Natural oxidation membrane on the silicon wafer was removed by the semiconductor cleaning solution SemicoClean23 purchased from Furuuti chemical company. Silazane compound diluted to 20% g/g with dibutylether was coated on the silicon wafer by the spin-coating technique. The stepwise thermal treatments under UV irradiation (max. 373K) induced the conversion of the silazane compound into SiO<sub>2</sub>. The thickness of obtained thin films was about 200-300 nm. Their XPS spectra were taken by Perkin Elmer PHI model 5600ci, in order to confirm the conversion of the coating films into SiO<sub>2</sub>. The surface morphology of the thin films was estimated by SII SPA300 atomic force microscopy.

Gold round electrodes were deposited on the top of the SiO<sub>2</sub> thin film through a metal mask. The area of gold electrode was  $7.85 \times 10^{-3}$  cm<sup>2</sup>. The I-V measurements were performed with a Keithley 4200-SCS parameter analyzer. The C-V measurement was performed by HP 4284A precision LCR meter at 1kHz. OFET with the SiO<sub>2</sub> thin film as a gate dielectric was fabricated using pentacene or P3HT as the semiconductive layer and the gold as the source and drain electrodes. The channel length was 20 µm and the channel width was 2 mm.

#### 3. Results and discussion

Fig. 1 shows XPS spectra of the SiO<sub>2</sub> thin film on a Si substrate. Upper profile shows a XPS spectrum for a thermally oxidized SiO<sub>2</sub> and lower shows solution processed SiO<sub>2</sub> thin film fabricated in this work. Three typical peaks assigned to the photoelectron from O1s, Si2s and Si2p were observed at 535, 155 and 105 eV, respectively. The chemical composition was estimated to Si:O=1:2.09 for the solution processed SiO<sub>2</sub> thin film. There were no differences on their binding energy and peak intensity, indicating that the solution processed SiO<sub>2</sub> thin film prepared in this work was stoichiometrically equivalent to the thermal oxidized SiO<sub>2</sub> thin film.

The resistivity of the solution processed SiO<sub>2</sub> thin film was estimated to the order of  $10^{13} \Omega \text{cm}$ . The breakdown was not found below the electric field strength 5 MV/cm. A similar measurement was performed for a thermally oxidized SiO<sub>2</sub> thin film. The resistivity was estimated to the order of  $10^{14} \Omega \text{cm}$  and the breakdown was observed at 8MV/cm. It was found that the resistivity of the solution processed SiO<sub>2</sub> thin film was 10 times lower than that of thermally oxidized SiO<sub>2</sub> thin films.

Table 1 shows the electronic parameters of the  $SiO_2$  thin films fabricated by various techniques. In order to employ the  $SiO_2$  thin film as a gate dielectric for the OFET, it is required to have extreme smooth surface. The surface of thermal oxidized  $SiO_2$  thin film is extreme smooth. However,  $SiO_2$  thin films obtained by CVD and sol-gel technique have a poor smoothness. On the other hand, it was found that the surface of solution processed  $SiO_2$  thin film prepared in this work had the smooth surface as same order with the thermal oxidized  $SiO_2$ .

Fig. 2 shows  $I_d-V_{ds}$  characteristics for pentacene OFET fabricated using solution processed SiO<sub>2</sub> as a gate dielectric. The field effect mobility was estimated as 0.364 cm<sup>2</sup>/Vs. The field effect mobility of pentacene OFET using thermally oxidized SiO<sub>2</sub> as a gate dielectric was estimated to 0.296 cm<sup>2</sup>/Vs from the similar measurement. These results indicated that the electronic performance of OFET using solution processed SiO<sub>2</sub> thin film as a gate dielectric was comparable to that using thermally oxidized SiO<sub>2</sub> thin film, though the resistivity of the solution process SiO<sub>2</sub> thin film was 10 times lower than that of thermally oxidized SiO<sub>2</sub> thin films.

# 4. Conclusions

We were succeeded to prepare SiO<sub>2</sub> thin film from the silazane compound by low temperature solution process. Obtained SiO<sub>2</sub> thin film had a high resistivity in the order of  $10^{13}$  Ωcm was 10 times lower than the thermally oxidized SiO<sub>2</sub> thin film. The OFET using solution process SiO<sub>2</sub> thin film was comparable to that using thermally oxidized SiO<sub>2</sub> thin film, indicating that the solution processed SiO<sub>2</sub> thin film was such useful for th2 gate insulator of OFET as the thermally oxidized SiO<sub>2</sub> thin film.

# References

- J. A. Rogers, Z. Bao, A. Dodabalapur and A. Makhija, IEEE Electron Device Lett. 21 (2000) 3.
- [2] M. Matters, D. M. de Leeuw, M. J. C. M. Vissenberg, C. M. Hart, P. T. Herwig, T. Geuns, C. M. J. Mutsaers and C. J. Drury, Opt. Mater. **12** (1999) 189.
- [3] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl and J. West, Appl. Phys. Lett. 80 (2002) 1088.

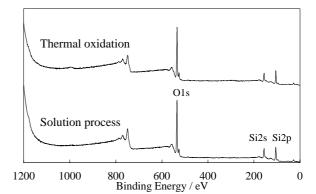


Fig. 1 XPS spectra of SiO<sub>2</sub> prepared by thermally oxidation (upper) and low temperature solution process (lower).

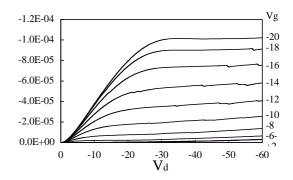


Fig. 2  $I_{drain}$ - $V_{source-drain}$  characteristics of pentacene OFET fabricated by using solution processed SiO<sub>2</sub> gate insulator.

Preparation Method	Temperatur e / K	RMS / nm	Field Effect Mobility / cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup>	Resistivit y / Ωcm	Dielectric Strength / MVcm <sup>-</sup>
Thermal Oxidation	>1223	0.139	0.296	~10 <sup>14</sup>	~8.0
Sputter	573	0.172	-	-	-
Thermal CVD	1173	0.916	-	-	-
Sol-gel	773	0.921	-	-	-
Solution Process (This Work)	<373	0.346	0.364	~10 <sup>13</sup>	>5.0

Table 1. Preparation temperature, surface roughness and electronic parameters of several SiO<sub>2</sub> thin films prepared by various techniques.