

High performance 0.1 μ m GaAs PHEMT with Si pulse doped cap layer for 77GHz car radar applications

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1. Introduction

The most commonly used frequencies in W-band transceiver systems are 77GHz and 94GHz. Recently, the 77GHz automotive car radars became more popular and power amplifiers were also designed and fabricated using 0.1 μ m gate-length GaAs PHEMT for these radar systems [1]-[3]. Therefore, Ohmic contact resistance is more important as the gate length is approaching to 0.1 μ m. GaAs PHEMT with InGaAs layer inserted the cap layer has been reported [4].

In this work, we present the 0.1 μ m GaAs PHEMT with InGaAs and Si pulse doped cap layer to improve ohmic contact, which demonstrated an ohmic contact resistance of 0.07 Ω -mm.

2. Epi-structure with Si pulse doped cap layer

This work deals with the double Si pulse doped Al_{0.22}GaAs/In_{0.22}GaAs PHEMT grown by molecular beam epitaxy (MBE) on a GaAs substrate, yielding a mobility of 5,650cm²/V-s and a sheet carrier density of 4x10¹²/cm² at 300K. To get lower ohmic contact resistance, we adopted the cap layer consisted of InGaAs contact layer and Si pulse dope donor layer. The cap layer was grown sequentially : 20nm Si doped (1x10¹⁸cm⁻³) GaAs layer, 12nm Si doped (6x10¹⁸cm⁻³) GaAs layer, Si pulse dope (6x10¹²cm⁻²) layer, and 8nm Si doped (3x10¹⁹cm⁻³) InGaAs contact layer. A schematic cross-section of the epitaxial structure is shown in Fig.1.

3. Process of 0.1 μ m gate length GaAs PHEMT

Devices were mesa isolated with a phosphoric etchant. The ohmic patterns were printed by photo lithography, at which time the alignment marks for the subsequent e-beam lithography were also formed. As the gate length is reduced to 0.1 μ m, ohmic contact resistance is required to be less than 0.1 Ω -mm. Ni/Ge/Au/Ni/Ag/Au ohmic contacts were deposited and alloyed by rapid thermal anneal at 440°C for 30s. The ohmic contact resistance was as small as 0.07 Ω -mm. Sheet resistance was 158 Ω /□.

Wide recess was performed by time controlled wet etchant. And the Si₃N₄ 300Å as a passivation layer was deposited on devices by Remote PECVD. The 0.1 μ m T-gates were defined by electron beam lithography using ZEP/PMGI/ZEP tri-layer and double exposure/double develop[5]. SEM photograph of tri-layer is shown in Fig. 2. After the definition of T-gate, Si₃N₄ layer was reactive

ion etched (RIE) in SF₆/Ar. The cap layer was etched using selective wet etchant (solution of Citric acid and peroxide), and Ti/Pt/Au gate metallization was evaporated [6]. SEM photograph of T-gate is shown in Fig. 3.

0.1- μ m GaAs PHEMTs were characterized on wafer for DC and RF performance. The DC I-V characteristics are shown in Fig. 4. Source resistance (R_s) is reduction of 20% compared to that of device without InGaAs and Si pulse dope donor in cap layer. This device exhibits a typical gate to drain breakdown voltage of -5.7V, peak dc transconductance of 620mS/mm and maximum drain current of 730mA/mm. The DC transconductance is shown in Fig. 5. Small signal S-parameters were measured from 1GHz to 110GHz. The RF characteristics are shown in Fig. 6. Unit current gain frequency f_T of 140GHz (V_{DS}=1.2V) and maximum oscillation frequency f_{max} of 265GHz (V_{DS}=2V) were extrapolated from the H₂₁ and the MAG, respectively [Fig.6].

In _{0.22} GaAs	Cap	3X10 ¹⁹ cm ⁻³	80Å
δ -doping		6X10 ¹² cm ⁻²	
GaAs	Cap	6X10 ¹⁸ cm ⁻³	120Å
GaAs	Cap	1X10 ¹⁸ cm ⁻³	200Å
Al _{0.22} GaAs	Barrier	i	220Å
δ -doping			
Al _{0.22} GaAs	Spacer	i	30Å
In _{0.22} GaAs	Channel	i	120Å
Al _{0.22} GaAs	Spacer	i	40Å
δ -doping			
Al _{0.22} GaAs	Barrier	i	750Å
GaAs/ Al _{0.22} GaAs	Buffer	i	3500Å
Substrate : GaAs S.I.			

Fig. 1. Schematic of GaAs PHEMT epi structure with Si pulse doped cap layer

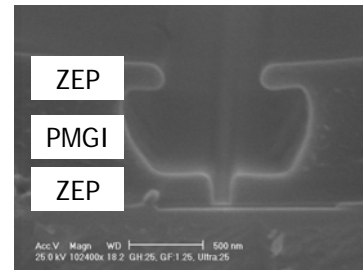


Fig. 2. SEM photograph of ZEP/PMGI/ZEP tri-layer

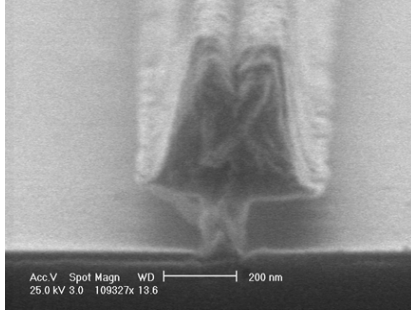


Fig. 3. SEM photograph of 0.1 μm T-gate

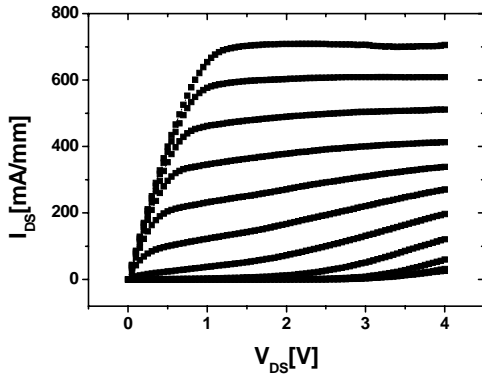


Fig. 4. DC I-V characteristics of 0.1x 50 μm^2 GaAs PHEMT with Si pulse doped cap layer : $V_{GS} = -1.6\text{V}$ to 0.4 step 0.2V step.

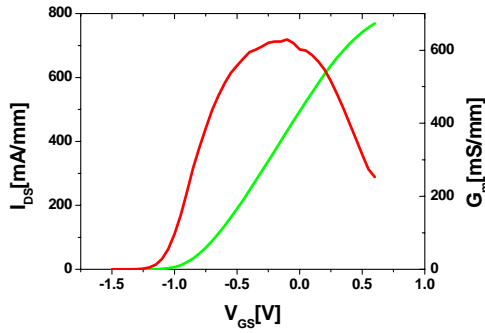


Fig. 5. DC transconductance characteristics of 0.1x 50 μm^2 GaAs PHEMT with Si pulse doped cap layer, $V_{DS}=1\text{V}$

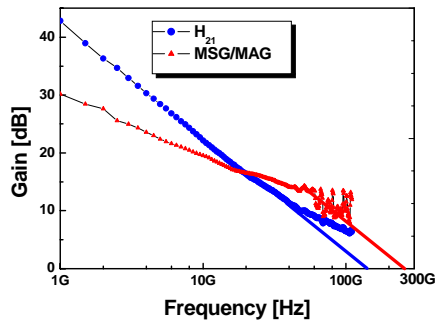


Fig. 6. RF characteristics of 0.1x 50 μm^2 GaAs PHEMT : f_T

of 140GHz ($V_{DS}=1.2\text{V}$) & f_{max} of 260GHz ($V_{DS}=2\text{V}$) was extrapolated from the H_{21} and the MAG

3. Conclusions

In this paper, 0.1 μm T-gates $\text{Al}_{0.22}\text{GaAs}/\text{In}_{0.22}\text{GaAs}$ PHEMTs with Si pulse doped cap layer have been successfully fabricated. The ohmic contact resistance was as small as $0.07\Omega\text{-mm}$, in consequence the maximum saturated drain current (I_{DS}) was about 730mA/mm. This devices showed good DC and microwave performance such as peak G_m of 620mS/mm, peak f_T of 140GHz and f_{max} of 265GHz. This is sufficient performance to apply to power amplifier for automotive car radar MMICs.

Acknowledgements

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References

- [1] H. Wang, *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2 pp. 419-421 (1995).
- [2] M. Aust, *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 12-15 (1995).
- [3] H. Y. Chang, *IEEE Microwave and Wireless Components Lett.*, vol.12, pp. 143-145 (2003).
- [4] S. Makioka, *IEEE Trans. Electron Devices*, vol. 48, pp. 1510-1514 (2001)
- [5] A.S.Wakita, *Journal. Vac. Sci. Technol. B*13(6)p2725-2728 (1995)
- [6] X. Hue, *Journal. Vac. Sci. Technol. B* 16(5) pp. 2675-2679 (1998)