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InGaP/InGaAs DCFETs with Drain and Source Recess Process

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1. Introduction

Doped-channel FETs (DCFETs) have demonstrated better device linearity, higher current density, and higher gate breakdown as well as higher turn-on voltages compared to HEMTs and MESFETs [1]. However, the main drawback of DCFETs is the high contact and sheet resistances of devices in the undoped Schottky access region between alloyed contact and gate electrode, which results in an increasing saturation voltage as well as thermal noise [2].

In this study, we proposed a drain-source ohmic contact recess doped-channel InGaP/InGaAs FET's (OR-DCFETs), and compared it with the conventional process in terms of dc, rf and power performances. The ohmic recess process can reduce the parasitic ohmic contact resistance, which cause by an undoped Schottky layer, and therefore, improve the device performance.

2. Device design

The OR-DCFETs and conventional DCFET structures, shown in Fig. 1, were grown in a Riber-32p molecular beam epitaxy (MBE) system on (100)-oriented semi-insulating GaAs substrate.

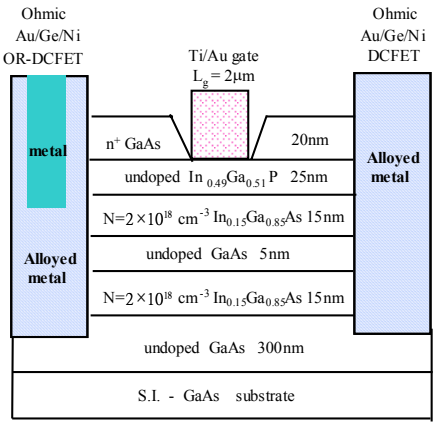

Fig. 1 The cross section of OR-DCFETs and DCFETs

Here, double doped channel structures have been used for better device performances [3]. The process of these two structures are all the same except a ohmic recessed process on OR-DCFETs to reduce the undoped schottky layer alloy metal resistance. The threshold voltages for both devices are –2 V. The drain-to-source current (I_{DS}) against voltage (V_{DS}) characteristics with 2 μm-long gate devices were shown in Fig. 2.

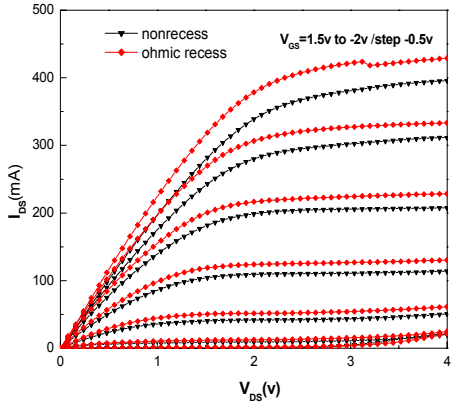

Fig.2 I_{DS}-V_{DS} characteristics of OR-DCFET/DCFET

It is obvious that the ohmic contact resistances of OR-DCFETs are improved by the ohmic recess design. Fig.3 shows the transconductance (g_m), I_{DS}-V_{GS} transfer characteristics. Both devices have the same g_m of 200mS/mm. We express the FETs I_{DS}-V_{GS} curves by a 6th order polynomial form to describe the output characteristics as following [1], and the an's are listed in Table 1.

$$I_{ds} = a_0+a_1V_{gs}+ a_2V_{gs}^2 + a_3V_{gs}^3 + a_4V_{gs}^4 + a_5V_{gs}^5 + a_6V_{gs}^6 \quad (1)$$

where an's are independent variables, which can determine the linearity associated with I_{DS}-V_{GS} transfer characteristics. In table 1, we find that the

values an's/a_1 for OR-DCFETs were much smaller than those for DCFETs. Therefore, higher linearity power performances can be expected for the OR-DCFETs by suppressing the 3rd (or higher)-order inter-modulation. A wide and uniform g_m distribution of OR-DCFETs, as compared with DCFETs can be also observedin Fig. 3. The maximum drain current (gate voltage swing for 90% g_m) is 500 mA/mm (1.5V) for OR-DCFETs, and 460 mA/mm (1.2V) for DCFETs, respectively.

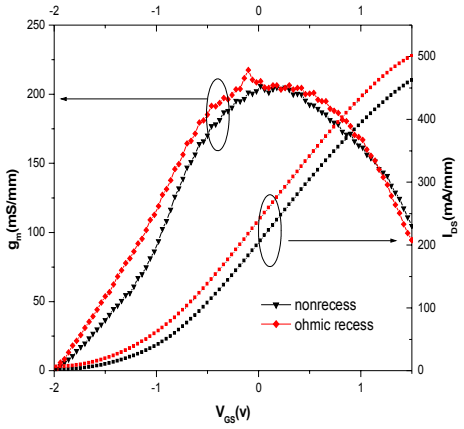

Fig.3 V_{gs}-g_m, I_{ds} characteristics of OR-DCFET and DCFET

an	a0	a1	a2/a1	a3/a1	a4/a1	a5/a1	a6/a1
DCFET	202.03	204.83	0.082	-0.1614	-0.012	0.0206	0.004
OR-DCFET	237.08	210.76	0.057	-0.1283	-0.008	0.0109	0.0019

Table 1.Compare of harmonic distortion factors between OR-DCFET and DCFET

Microwave on-wafer S-parameters for 2.0 μm-long gate devices were measured by a HP-8510 network analyzer. A f_T and (f_{max}) of 5.5 GHz (18 GHz) for D-DCFETs, 5.2 GHz (17Hz) for DCFETs were obtained at V_{ds}=2.5 V, shown in Fig. 4, respectively. For DCFETs, a decrease of both f_T and f_{max} started to occur at I_{ds} > 250mA/mm. However, no significant performance reduction was observed for OR-DCFETs till I_{ds} = 400mA/mm. These microwave behaviors are similar to dc characteristics. Microwave power performances were characterized at V_{ds} = 2.5V under a 1.9 GHz operation for the gate dimension of 2×50 μm^2 devices. Linear power gains were 11 dB for both devices. The maximum output power and PAE were 7.6 dBm (115 mW/mm) and 13 % for O-DCFETs, and 7 dBm (100 mW/mm) and 10.2 % for DCFETs, respectively. Although the performances are not so outstanding for these devices, better performances can be achieved by using shorter channel devices.

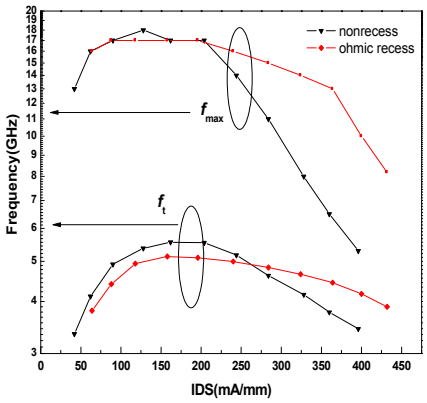

Fig. 4 I_{DS} dependence of f_T, and f_{max} for OR-DCFET and DCFET

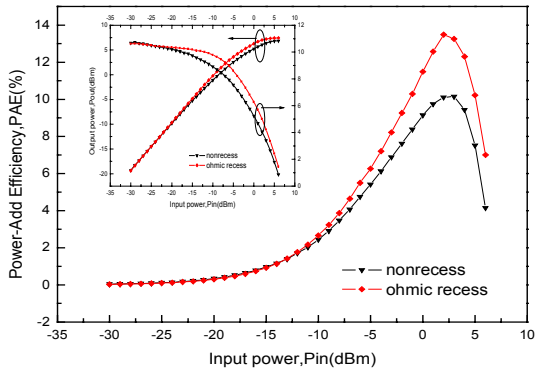

Fig. 5 Power Performance comparison between OR-DCFET and DCFET

4. Conclusions

DCFETs with ohmic recess (OR-DCFET) process have been proposed and demonstrated improved characteristics than the conventional DCFETs devices. One can use this technology for sub-μm device for better performances.

References

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