Process Realization for 3-D ICs using Fine Pitch Through Silicon Vias

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1. Introduction

The motivation for developing 3-D IC stacking using through silicon vias (TSVs) for Z-axis connections has been previously discussed [1, 2]. This paper describes the progress made at the University of Arkansas in developing a process for creating 4 µm diameter TSVs on 20 µm pitch in wafers subsequently thinned to 20 µm.

This work is part of the larger DARPA VISA program (Vertically Integrated Sensor Arrays) whose goal is to provide per-pixel image processing by attaching a stack of several silicon processing elements to the back of a large image sensor, resulting in extremely dense signal processing hardware.

2. Via Formation

The first step in forming the TSVs is to create a via that is 4-6 um in diameter and 15-20 microns deep in the silicon. Both conventional reactive ion etching (RIE), and Inductively Coupled Plasma (ICP) utilizing the Bosch process are being developed. The desired via must have slightly tapered sidewalls, so that subsequent deposition of the oxide insulator and metal barrier and seed layers will achieve uniform coverage. However, the vias must not taper too much, which would create too small a via at the bottom and could limit the desired depth, as shown in Figure 1a.

Normally, ICP is used to produce absolutely straight side walls, but published papers have indicated that tapered sidewalls can be produced by appropriate modification of process parameters during the etch step [3, 4]. The process is under development.

Meanwhile the RIE process has produced reasonably good vias, as shown in Figure 1b. These vias were produced using a PlasmaTherm SLR 720 system (currently known as Unaxis) with the conditions as follows: SF$_6$ 40 sccm, O$_2$ 35 sccm, power 180 W, pressure 100 mT, and time 30 minutes.

3. Insulation and Seed Layer Deposition

Chemical vapor deposition (CVD) is used to deposit SiO$_2$ in order to insulate the subsequent via metal from the surrounding silicon. The CVD process was carried out in a PlasmaTherm SLR 730 using the parameters as follows: SiH$_4$ 85 sccm, N$_2$O 450 sccm, N$_2$ 450 sccm, Power 55 W at 13.5 MHz. Deposition at 325°C for 5.5 minutes resulted in a uniform layer of SiO$_2$.5 µm thick.

A metal layer consisting of a barrier/adhesion layer and a copper seed layer is then deposited. Physical vapor deposition (sputtering) is used to deposit these layers. Sputtering has proven effective if the via geometry is properly controlled, as shown in Figure 2. The barrier layer consisted of a 1000Å layer of titanium, and was produced in an XM-8 sputtering system with Argon at 5mT and 2500 watts of power for 11 seconds. The seed layer is 3150 Å of copper deposited in the same sputtering system using 3000 watts of power and 5mT pressure for 20 seconds.

4. Copper Plating

Following seed layer deposition, the via is plated with copper until solid, with no voids. Reverse pulse plating is used. In this technique, copper is not deposited continuously; plating current is applied in short pulses to give plating bath constituents time to reestablish an adequate concentration at the plated surface. Periodically, reverse current pulses are applied to remove material from more thickly plated regions. Careful control of bath chemistry, pulse current, time, and frequency are used to optimize results [5].
In order to ensure that plating solution continuously reaches the sidewall area of the vias, a form of fountain plating is used. A special “shower head” has been designed to direct many jets of plating solution at the surface to be plated. The streams of plating solution pass through a perforated anode before impinging on the wafer surface.

The plating solution used is CUBATH SC from Enthone Inc. It contains 33.5 average oz/gal of copper sulfate and 8.5 average oz/gal of copper upon delivery. Additives, also obtained from Enthone, are added to the solution in the amount of 10 mL/L. The anodes used are 99.99% pure copper with 0.04 to 0.06% phosphorous.

Once the anodes are conditioned, they are placed in the plating bath with the wafer and are ready to plate. The current density used is 2.0mA/cm². The plating profile is as follows: 30ms forward / 1.5 ms reverse / 30 ms off. The result for a partially plated via is shown in Figure 3.

5. Wafer Attachment
After forming the solid copper via plugs, the processed wafer must be attached to a carrier wafer for thinning. A film of LCP (liquid crystal polymer) material, 50 µm thick, with a CTE of 8, is laminated at 290°C and 10 tons of pressure between the processed and carrier wafers. Total wafer planarity of 3 µm is obtained.

6. Wafer Thinning
After attachment the wafer was ground from 370 µm to 50 µm using 9 µm alumina powder for 2 hours, and polished using 0.3 µm alumina powder for 1 hour; the final thickness was 40 µm. The planarity obtained is ± 4 µm. We are working to improve the bonding technique to obtain better planarity.

Next, spin spray etching is used to remove the mechanical damage in the thinned wafer. The spin spray etch machine used is the Laurell WS-400A-6TFM-FULL. The initial results using the system as shipped showed poor planarity, so a new large showerhead was fabricated. After adjustment of the showerhead hole pattern, the wafer was thinned from 40 µm to 30 µm and the planarity was ± 5 µm (2 µm additional variation from spin spray etching.)

This wet etching process is used to reduce the thickness of the wafer to within a few microns of the blind vias. Then the wafer is again placed in the STS system and silicon is removed by RIE. Because of process selectivity, the vias, coated with silicon dioxide, are left standing proud of the surface. The wafer is then ready for backside processing.

7. Backside Processing and Testing
The backside processing steps create via connection pads to allow for eventual system assembly. After the wafer has been thinned, it is placed in the PECVD system where an oxide layer is deposited. Using photolithography and wet etching, the bottoms of the copper vias are exposed. Copper pattern plating over a seed and barrier layer is then used to create bottom connecting pads.

To test the process, wafers will be probed from the backside. Additional masks for front and back metal will define test structures for measuring via chain continuity and resistance, four point probe via resistance, and via isolation at DC. These tests can be made with the wafer still attached to the carrier wafer.

8. Conclusions
This paper has described the process development under way for TSVs as a means to perform Z-axis interconnection among several stacked silicon slices. The TSV process is elaborate, and is not yet completely worked out, but it shows great promise as a way to achieve architectures in silicon impossible with any other method.

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References

Figure 3. Pulse plating (partial) for bottom up via fill.

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