Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 276-277

F-3-2

Application of High Reliable Silicon Thru-Via to Image Sensor CSP

Kojiro Kameyama, Yoshio Okayama, Mitsuo Umemoto, Akira Suzuki,
Hiroshi Terao, Masataka Hoshino, and Kenji Takahashi

Association of Super-Advanced Electronic Technologies (ASET)
10F, Time 24 Bulid., 2-45 Aomi, Kotou-ku, Tokyo, 135-8073. JAPAN
Phone: +81-3-5531-0120, Fax: +81-3-5531-0122, E-mail: KAME070710@sanyo.co.jp

1. Introduction

Recently, ultra-high density packaging technology that is required for mobile equipment, ubiquitous computing device, and so on is becoming very important. Three-dimensional chip stacking which has vertical interconnections through the silicon chip has been recognized as the most effective technique to realize the system integration in terms of thin, light, low power consumption and high performance.

In the Japanese national project of "Electronic System Integration", the 3D chip stacking technology with ultra fine pitch vertical interconnection using silicon thru-via has been developed [1-3]. However, very few studies about commercially available chips have been presented [4].

In this paper, we demonstrate the application of silicon thru-via technology to charge coupled device (CCD) image sensor wafers which were assembled into commercially available CCD modules for built-in cameras of cellular phones, and proved the thru-via technology had high reliability and yield levels as volume production.

2. Experiment

We applied the thru-via to a chip scale package (CSP) of a CCD image sensor without chip. The active surface of an image sensor wafer should be covered by protection layers. Thus, we adopted a structure that the wafer surface was covered with a glass wafer and the silicon thru-via makes vertical interconnection between back of Al pads and solder balls formed on back of the wafer. Fig. 1 shows the structure of a CCD image sensor CSP with the thru-vias.

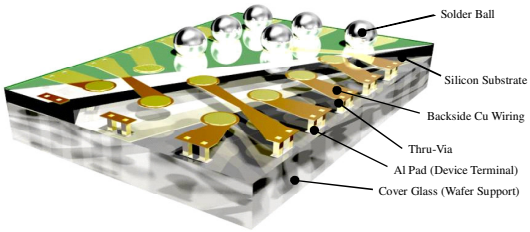

Fig. 1 Structure of image sensor module.

The process flow diagram of fabricating thru-vias is shown in Fig. 2 A wafer on which CCD device fabricated was attached to a glass wafer, which also worked as a support layer, thinned to 130 µm by grinding and wet etching. Photo resist patterned with i-line aligner and high-speed silicon etching fabricated the thru-vias. Then, SiO_2 layer remaining at bottom of via was etched, SiO_2 deposited by chemical vapor deposition (CVD) for insulating thru-vias with silicon, and SiO_2 at bottom was etched again. Next, a barrier metal (TiN) and seed metal (Cu) were deposited by metal organic CVD (MOCVD) and 5 µm thick of Cu was electroplated.

After that, Cu was patterned as backside wiring by wet etching, coated with solder resist and solder balls were located at prescribed position. Finally, the wafer was diced into CSP.

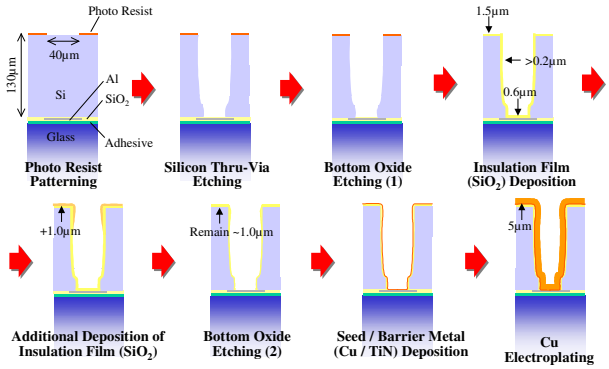

Fig. 2 Process flow diagram of fabricating thru-via.

3. Results and Discussion

Process Integration for CCD devices

Fig. 3 shows a cross-sectional micrograph of a thru-via fabricated in this study. It is shown that an Al pad is connected with the backside wiring by Cu formed on the sidewall and bottom of a thru-via.

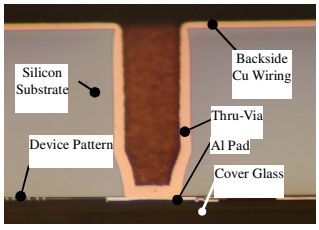

Fig. 3 Cross-sectional micrograph of a thru-via.

Major technical challenges for this application were control of silicon thru-via etching and low temperature process integration. In addition, to indicate that this technology would be commercially available in terms of cost, we have developed the SiO_2 etching of via bottom without any mask and high speed Cu plating with a conformal coverage.

Silicon etching is processed by magnetron reactive ion etching (RIE) with SF_6 and O_2 gas. As a result of experiments of varying etching conditions, it was found that the notching shape (etching intrusion to the sidewall of the silicon) formed at the bottom of the thru-via was improved by 2 step etching by power controlling.

Low temperature process integration, especially SiO_2-CVD

and TiN/Cu-MOCVD processes, was required to suppress thermal degradation of organic materials on the CCD wafers. According to the evaluation of the durable temperature of the CCD wafer, the amount of degas from the wafer, film properties, and deposition rates, it was found that 170 °C was the maximum temperature to process the wafer and a good integration was achieved at the temperature.

Fig. 4 shows the results of the structural simulation for estimating the maximum stress in the Cu, Si and SiO_2. The simulation was conducted under the conditions that stress was free at 125 °C and simulated temperature was 25 °C. The results indicated that the maximum stresses of Cu, Si and SiO_2 were 130 MPa, 200 MPa and 100 MPa, respectively. Because the maximum stress is below the fracture limit of SiO_2, the structure including Cu electroplated film is expected to be highly reliable against thermal cyclic test.

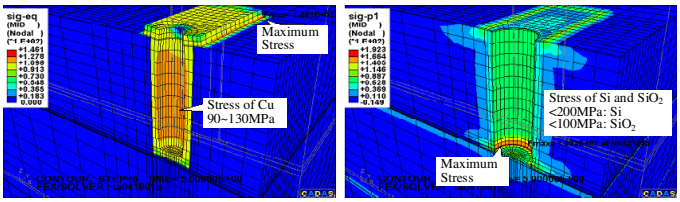

Fig. 4 Structural analysis of a thru-via.

Characteristics of Thru-Via

In order to investigate the electrical integrity of thru-vias and back wiring of the CSP, thru-via chain tests were conducted. The test vehicle had thru-vias of 30 and 40 µm in size in one wafer, and 2 to 16 vias were connected to form chains.

Figure 5 shows the test results. The electrical yield of the chains was as high as 99 %. In addition, the electrical resistance of the via was below 50 mΩ which was nearly equal to the theoretical value. Thus, it is considered that thru-via technology is in a ready for manufacturing level.

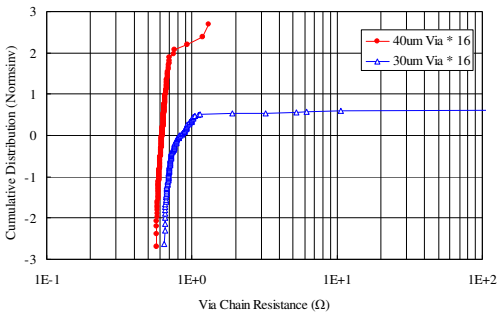

Fig. 5 Thru-via chain resistance within a wafer.

Meanwhile, the 30-µm-size via resistance was very higher at the outer side of the wafer. It is considered that the Si etching condition was adjusted to 40-µm-via process and non-uniformity of etching rate within the wafer became critical.

Reliability of Thru-Via

It has been said that CSP, especially WL-CSP, is less reliable in package reliability tests than the ordinary resin molded packages. Particularly, temperature cyclic tests (TCT) is the most severe one in the package reliability tests. Thus, we applied the TCT to the CCD package with the novel thru-via structure. The temperature range was from -25 °C to 125 °C, 2 cycles / hour and the sample number was 49. Electrical resistance change larger than 10 % of the initial value was classified as failure.

As the results, 1000 cycles were completed without increase of the via chain resistance as shown in Table 1. Even though the decrease of resistance was found, it was proven that the initial resistance was higher than theoretical value because of the existence of several nm of an oxidized Aluminum layer formed by etching or wet cleaning process. It is considered that the high resistance layer is broken by the stress in the TCT, so resistance is decreasing. Our lately fabricated samples which are controlled of the formation of the oxidized layer indicate very low resistance as well as calculated. In addition, no short failure was shown in the TCT.

Performance of Camera Module

With the CCD image sensor CSP using thru-via, CCD camera modules for cellular phone were assembled. Fig. 6 (a) shows the camera module, which is assembled on a PWB and has a lens holder, a CCD driver chip, a DSP chip, and so on. The module except for the CCD chip was the same as a commercial product that was produced in a large volume.

Then, the performance of the camera module was evaluated. Fig. 6 (b) shows a photograph taken by the module. It is found that the imaging quality of the module with the CCD image sensor CSP using thru-via is equal to that of the commercial module without thru-via technology.

(a) **(b)**

Fig. 6 (a) Image sensor module with thru-via CSP, (b) Photograph taken by the module.

4. Conclusions

The silicon thru-via technology was applied to an image sensor CSP, and proved that has high reliability and yield enough to apply to commercial production. It becomes a great milestone in practical use for 3D packaging and silicon thru-via technology.

Acknowledgements

This work was performed under the management of ASET in the METI's R&D Program supported by NEDO.

References

[1] K. Takahashi et al., *Jpn. J.Appl. Phys.*, **40**(4B), 3032 (2001).

[2] K. Takahashi et al., submitted to *54th Electron. Components and Technol. Conf.*, Las Vegas, NV, Jun. 2004.

[3] M. Umemoto et al., submitted to *54th Electron. Components and Technol. Conf.*, Las Vegas, NV, Jun. 2004.

[4] K. W. Lee et al., *Jpn. J.Appl. Phys.*, **39**(4B), 2473 (2000).