Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 280-281

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Connection Test of Area Bump Using Active-Matrix Switches

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1. Introduction

The three dimensional (3D) chip-stacking technology is attracting a great deal of attention for realizing advanced high-speed, compact, and highly functional electronic systems.[1−3] In order to realize the 3D stacked-chip system, the development of the area-bump bonding technology is certainly required. For the development and the quality control of the bonding technology, test of bump connections is necessary. The connection test becomes important especially when the process margin of bonding process (the alignment margin, the parallelism between the chip holding tool and stage of bonding machine, the bump height deviation and so on) becomes small. Moreover, the test method which can be applied to high-density (below 20 μm in bump-pitch) large-number area-bumps is required for 3D stacked-chip system. The daisy chain of bump connections (Fig. 1) has been widely used to test bump connections. However, using this method, it is difficult to test the connection of individual bumps and investigate the distribution of bonding failure. Therefore, it takes long time to find causes of bonding failure and to develop bonding process.

In this paper, we propose a new test method which can test connection of individual bumps spread over the chip area. The method uses active-matrix of MOSFET switches. Figure 2 shows the schematic illustration of the bump connection test using active-matrix MOSFET switches. One of the bumps is electrically selected using the active-matrix and current-voltage characteristic between lower chip and upper chip is measured through the selected bump.

2. Experiment

Figure 3 shows the optical micrograph of upper and lower chips fabricated. The lower chip contains active-matrix together with LUT (Look Up Table) circuits which select a row and a column from matrix. The MOSFETs for active-matrix and LUT were fabricated using Al gate process. The gate length and gate width were 5 μm and 110 μm, respectively. The thickness of gate oxide was about 50 nm. Each matrix contains two MOSFET switches and one bump. The size of the matrix fabricated was 10 × 10. The upper chip simply contains a 10 × 10 array of bumps. In addition to the bump array, the upper chip contains additional 4 bumps at each corner of the chip, which are electrically connected to bump array through the under bump metallurgy (UBM). These additional bumps were used to measured the current-voltage characteristic. Bumps were formed using the so-called UV-LIGA technique which combined UV lithography with Au electroplating. Bump size was 110 μm × 110 μm × 9 μm.

Figure 4 shows the process step of chip bonding between upper chip and lower chip: (a) The resin was dropped on the center of the chip. (b) The alignment was performed. (c) The upper chip was pressed against the lower chip and two chips were heated to bond the bumps and cure the resin. Chip bonding was carried out using a flip-chip bonder. Chip bonding condition was as follows; pressing load: 10 kgf or 3 kgf, temperature (lower chip side): 100°C, temperature (upper chip side): 200°C, bonding time: 20 sec, chip size: 2.5 × 2.5 mm^2.

3. Results and Discussion

Figure 5 shows two typical example of I-V characteristic measured through a bump connection selected by active-matrix. When the bonding of bump connection was successful (Fig. 5(a)), the output current I_{OUT} shows a typical I_D-V_G characteristic of a MOSFET. When a bump whose connection was failed is selected (Fig. 5(b)), the output current I_{OUT} did not appear.

Figures 6(a) and 6(b) show the spatial distributions of bonding failure of bump connection obtained for two pressing loads, 10 kgf and 3 kgf, respectively. The symbols "successful", "failed" and "unknown" represent "the bonding is successful", "the bonding is failed" and "the measurement is impossible because of the degradation of MOSFET", respectively. We find that there are few bonding failure when the pressing load is increased to 10 kgf while there appear many bonding failure when bonding was carried out under pressing load of 3 kgf. We also find that the position where the bonding failure appeared corresponds to where the resin was dropped. From these results, we can determine that, in this test bonding process, the cause of bonding failure is residual resin and the pressing load required for complete bonding is over 10 kgf.

4. Conclusion

A new method of bump connection test using active-matrix MOSFET switches was proposed. This method can determine the connection of individual bumps and, therefore, is useful to investigate the cause of bonding failure. This test method will contribute to the development and the quality control of the bonding technology.

Acknowledgment

This work is supported in part by Kitakyushu knowledge-based cluster project of the Ministry of Education, Culture, Sports, Science and Technology.

References

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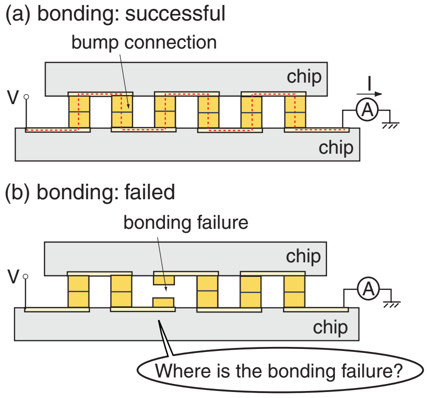

Fig. 1: The test of bump conncections using the daisy chain, which has been widely used. This method, however, is not able to identify the bump failed.

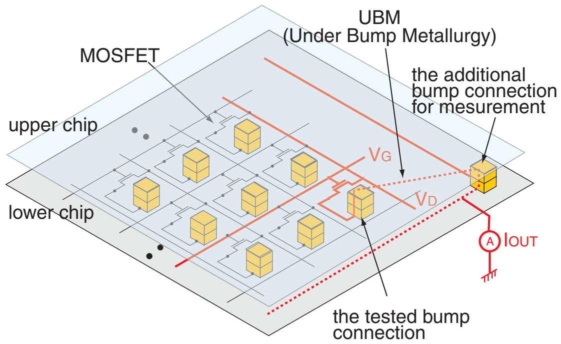

Fig. 2: The new method of bump conncection test using active-matrix of MOSFET switches.

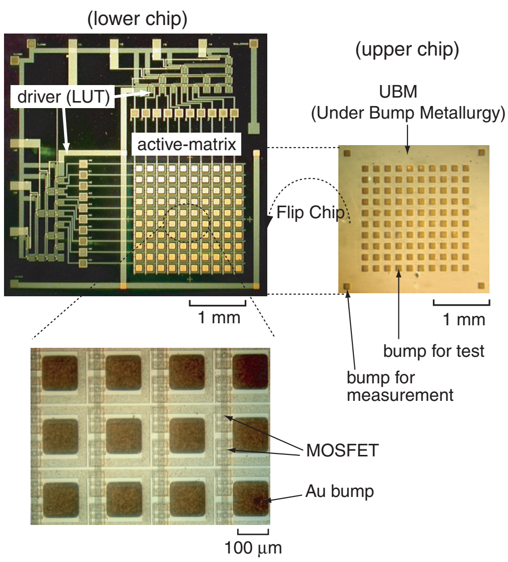

Fig. 3: The optical micrograph of test chips fabricated.

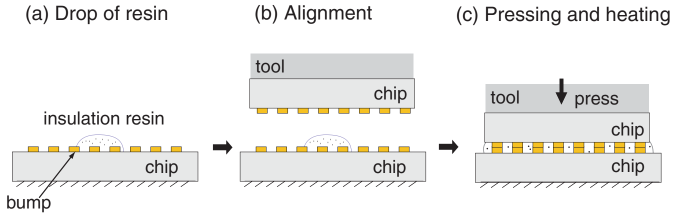

Fig. 4: The process steps of chip bonding with resin: (a) The resin was dropped on the center of the chip. (b) The alignment was performed. (c) The upper chip was pressed against the lower chip and two chips were heated to bond the bumps and cure the resin.

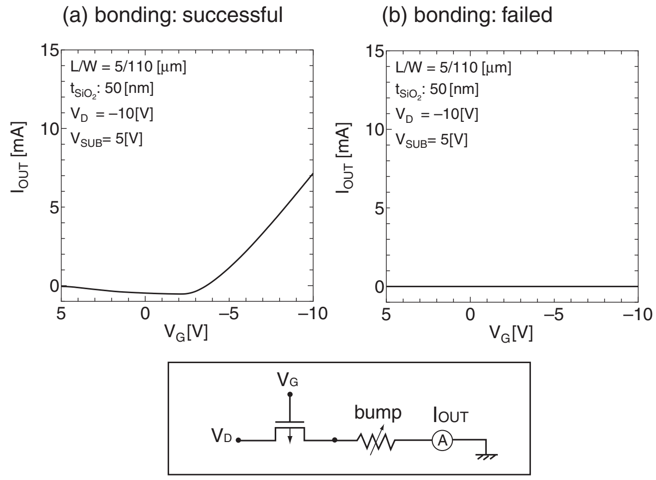

Fig. 5: Two typical examples of I-V characteristic measured through (a) successfully bonded bump and (b) bonding failed bump selected by the active-matrix.

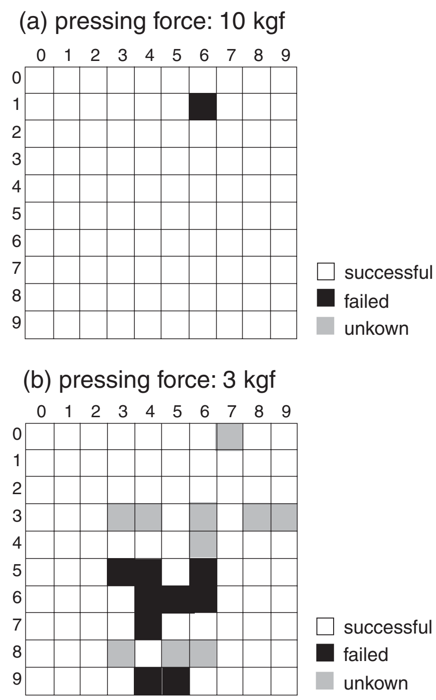

Fig. 6: The spatial distributions of bump bonding failure for the cases where bonding was carried out under pressing load of (a) 10 kgf and (b) 3 kgf.