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Wafer Level Package Integrated Functions

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1 Introduction

Thin-film Wafer-Level Packaging (WLP) technology offers the advantage of high precision, low temperature and low cost and has previously been used for the realization of high-Q off-chip passives and SiP based RF circuits and modules [1-2]. Besides the redistribution of bonding pads, thin film WLP offers novel opportunities to the functionality of ICs. First, it can fill the interconnect gap between the global on chip wiring and the board level interconnects providing fast interconnect lines [3]. Second, it offers possibilities for the integration of high quality RF passives, notably low loss transmission lines and high-quality inductors [4].

This paper focuses on the advantages of thin-film WLP technology for on-chip RF and RF/digital applications.

2 Thin-Film WLP for RF Applications

Inductors integrated in today's back-end (BEOL) Si processes have difficulties to meet the high performance specifications for future RF ICs [5] as they typically use a fairly resistive Al/Cu metallization to pattern the spiral and underpass. Furthermore, as the integration level increases, the metal thickness is typically thinned to decrease the achievable line pitch. This thinning of metal layers and their associated inter-layer dielectrics as process technologies advance, creates a fundamental problem for realizing high-Q inductors on-chip. Increasing the on-chip inductor performance may be done by replacing the conventional Al/SiO_2 technology with low-K materials and thick Cu metallization, however, thick Cu is not a standard BEOL process and the dielectric in-between the spiral and the lossy substrate is still relatively thin.

Thin film inductors realized above the passivation, on the other hand, make use of the availability of thick Cu metallizations and low-k dielectrics and improve as such the performance of the on-chip inductors significantly.

IMEC's WLP process has been realized on top of a 5 levels of metal (5LM) Cu/oxide BEOL using 20Ω.cm Si. The WLP inductors and transmission lines are realized on top of the passivation using two process flows (see Fig. 1 & Table 1). In flow-1, 5µm photo-BCB (benzo-cyclobutene, ε_r=2.65) (BCB-1) is deposited first, the electrical contacts to the underlying BEOL are opened using conventional photolithography. WLP-M1 (5µm Cu) directly connects to the top BEOL layer. BCB-2 protects WLP-M1 from oxidation; a Cu/Ni/Au top metal makes the flow compatible with wire bonding. The inductors and interconnects are preferably realized in WLP-M1; WLP-M2 may be used to create overpasses. In case flip chip bonding is used, WLP-M2 acts as UBM (under bump metallurgy) for the solder bumps.

As the aspect ratio of standard photo-BCB vias is <1:4, large vias are needed when the BCB-thickness is increased above 10µm. To keep the via size and pad capacitance small when the BCB-thickness is increased, a special high aspect ratio via (HARVi) is used in flow-2: first, a metal stud is plated on top of the BEOL, then BCB-1 is deposited. Due to planarization, only a thin BCB-layer is present on top of the HARVi, which is opened using conventional photolithography. A FIB cross-section of a flow-2 stack on top of M1-M5 is shown in Fig. 1.

The WLP transmission line performance is illustrated in Fig. 2 for 50Ω coplanar waveguides (CPW) (strip width 20µm, slot 10µm) and thin-film microstrip (TFML) realizations (10µm strip in flow-1, 30µm in flow-2). Losses as low as -0.1dB/mm @25GHz can be achieved.

The inductor layout parameters and performance are summarized in Table 2: Q_{max} in flow-2 is about 35% higher than those obtained in flow-1. The realization of the underpass also has a significant impact on the inductor performance as shown in Fig. 4: realizing the spiral in M5 with 20µm wide M4 underpass has Q_{max}=5, using WLP-M1 (flow-1) with 20µm wide M5 underpass increases Q_{max} to 16.5, putting a 30µm wide overpass in parallel with the underpass further increases Q_{max} to 21. A flow-2 version with WLP-M2 overpass and M5 underpass has a Q_{max} of 28.

Patterned ground shields decrease the substrate induced losses, hereby increasing the performance of the post-processed inductors. In this work, a patterned polysilicon ground shield has been used [6]. The impact on the inductor performance is shown in Fig. 5.

3 Thin-Film WLP for RF/Digital Applications

A schematic cross-section of IMEC's WLP-flow for RF/digital applications is shown in Fig. 6 [3]. Next to high quality RF components, low loss high speed interconnects may be realized in the WLP layers. Both interconnect configurations based on TFML with integrated Ta_2O_5 decoupling capacitors as well as the Integrated Meshed Power Ground System (IMPS) [7] can be realized.

In the IMPS topology (Fig. 7), the signal line is sandwiched between Power and Ground lines with identical but perpendicular wiring structures in the adjacent layers. The IMPS and TFML lines were designed to have a characteristic impedance of 50Ω.

As shown in Fig. 8, the WLP transmission line delay profile shows a near speed of light transmission from 600MHz on. It can also be observed that the simulated 70nm node upsized global interconnect delay strongly varies with frequency and exhibits a flat response only beyond 2GHz.

4 Conclusions

A thin-film WLP technology on top of a 5LM BEOL was presented providing novel opportunities for extended global wiring and passives at low cost. High-quality spiral inductors and transmission lines have been integrated.

References

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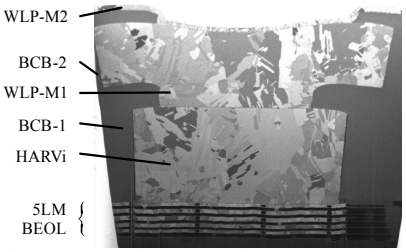

Fig. 1: Focussed Ion Beam (FIB) cross-section of the flow-2 (Table 1) "inductor above passivation"-layers on top of BEOL M1-M5.

	flow-1	flow-2
BCB-1	5 µm	16 µm
WLP-M1	5 µm	10 µm
BCB-2	8 µm	12 µm
WLP-M1 minimum width	5 µm	10 µm
WLP-M1 minimum spacing	5 µm	10 µm

Table 1: Realized flow-1 and flow-2 BCB & WLP-M1 thickness. The layer location is illustrated in Fig. 1.

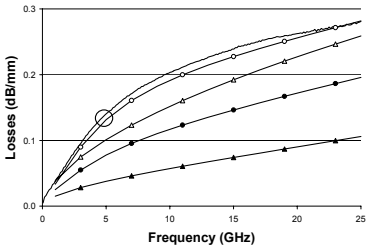

Fig. 2: Measured (-) 50Ω CPW loss (flow-1). Simulated (Ansoft HFSS) 50Ω CPW (flow-1 (-o-), flow-2 (-●-)) and TFML (flow-1 (-Δ-), flow-2 (-▲-)) loss.

	N	W (µm)	S (µm)	D_{in} (µm)	D_{out} (µm)	Area (mm^2)	Shield	Flow-1				Flow-2			
								L (nH)	Q_{max}	F_{Qmax} (GHz)	F_{res} (GHz)	L (nH)	Q_{max}	F_{Qmax} (GHz)	F_{res} (GHz)
L1	2.5	10	10	110	50	0.035	No	1.17	18.7	4.4	27	1.13	25	4.4	30
L2	3.5	10	10	110	50	0.049	No	2.28	16.2	2.6	16	2.18	22	2.9	18.5
L3	1.5	20	10	215	50	0.078	No	0.97	24.5	3.3	25.8	0.93	34	4.2	28.5
L4	2.5	20	10	215	50	0.110	No	2.35	20.6	1.5	13	2.25	28	2.1	15
L5	2.5	20	10	215	50	0.110	Yes	2.22	23.7	3.3	9	2.18	31.4	4.4	12
L6	4.5	20	10	215	50	0.192	No	7.11	16.9	0.8	5	6.9	23	1.2	6.5

Table 2: Layout parameters (see Fig. 3) and measured performance of the WLP inductors (F_{Qmax}: frequency at which Q is maximal): a WLP-M2 overpass and M5 underpass are used, substrate contacts at both ports. Q-factors are derived from measured S-parameters using $Q = imag(1/Y_{11})/real(1/Y_{11})$.

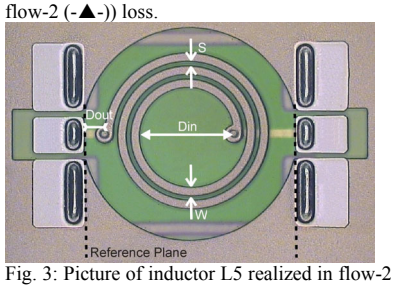

Fig. 3: Picture of inductor L5 realized in flow-2 with M5 underpass and patterned polysilicon ground shield. Meaning of layout parameters and inductor reference plane is also indicated.

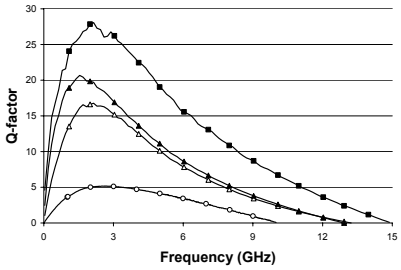

Fig. 4: Measured Q-factor of L4 realized in M5 with M4 underpass (-o-), flow-1 with M5 underpass (-Δ-) and added WLP-M2 overpass (-▲-), flow-2 with WLP-M2 over- and M5 underpass (-■-).

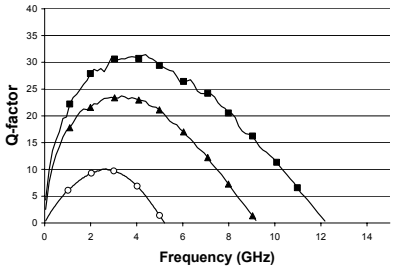

Fig. 5: Measured Q-factor of inductor L5 realized in M4//M5 with M3 underpass (-o-), flow-1 (-▲-) and flow-2 (-●-). A patterned polysilicon ground shield is present underneath the inductors.

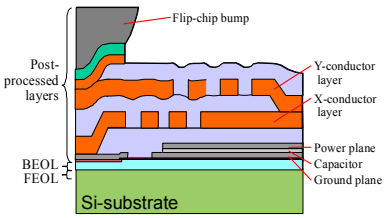

Fig. 6: Schematic cross-section of the WLP concept for the realization of high speed interconnects, inductors and power-ground decoupling capacitors.

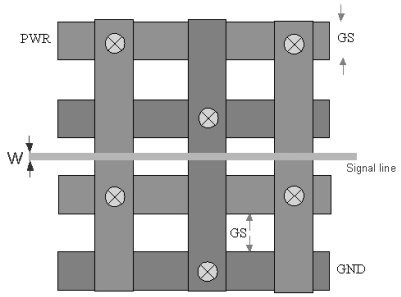

Fig. 7: Schematic representation of the IMPS geometry and design parameters.

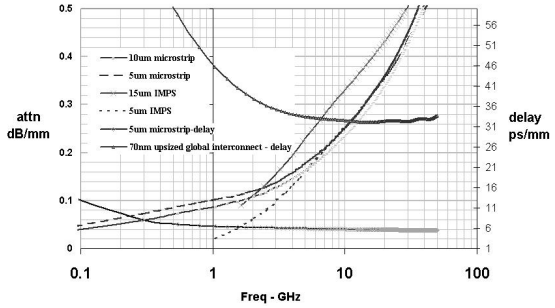

Fig. 8: Measured attenuation and delay as a function of frequency of microstrip and IMPS lines versus frequency realized in the WLP layers.