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On-chip Spiral Inductors Integrated with Wafer-Level Package

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***Abstract*— On-chip high-*Q* spiral inductors on Si substrate integrated with WLP have been successfully fabricated. The inductance *L* of 5.2 nH with the quality factor *Q* of 27.0 was obtained by a 3.5 turn rectangle spiral inductor with encapsulation layer at 2 GHz on the Si substrate, which had a resistivity of 4-6 Ωcm. In addition, the measured results of *Q* and *L* were well corresponded to the simulated values by HFSS and Sonnet. This technology realizes built-in high quality inductors in the IC package.**

1. Introduction

On-chip inductor integrated with CMOS circuit is one of the most important passive components for many RF systems [1]. The improvement in its performance such as precise inductance (L) with high quality factor (Q), high frequency at Q peak, high self-resonant frequency (f_{res}) and small device footprint are important.

This paper proposes that all on-chip inductors are integrated with wafer level package (WLP). The schematic illustration of the on-chip spiral inductors in WLP is shown in Fig. 1. This WLP structure consists of dual Cu electroplated layers, dual resin layers, an encapsulation layer and lead-free solder bumps. The embedding inductors are located between the second resin layer and the encapsulation layer in conjunction with WLP process. Accordingly, this technology has desirable features of: (1) having separated conductive lines by thick resin layer to reduce the induced eddy current in Si substrate; (2) being supported by thick electroplated low-resistive copper, Cu,; and (3) eliminating additional inductance from wire bonding. In addition, WLP technology has already achieved the thermal stabilization, high reliability and cost efficiency [2].

2. Structure and Fabrication Process

A variety of geometry was designed and analyzed by electromagnetic field simulators (HFSS and Sonnet). The main target of the design was to obtain L of 5 nH at 2 GHz in a 3.5 turn spiral inductor. Table I shows geometrical patterns and typical dimensions of the fabricated spiral inductors. A-type is a basic structure of the inductor, in which the coil pattern is away 20 μm from Si substrate by separating the first and the second resin layers. B-type is the same structure as A-type except for the resistivity (ρ) of Si substrate to compare with the substrate due to the eddy current loss between A-type and B-type.

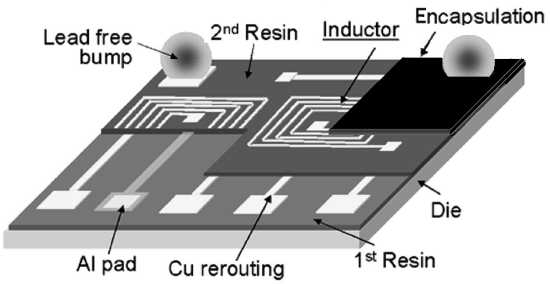

Fig. 1 Schematic illustration of on-chip spiral inductors in WLP.

Table I
Geometrical patterns and typical dimensions of the fabricated spiral inductors

	A	B
Number of turns (N)	2.5 – 5.5	
Si resistivity (Ωcm)	4 - 6	> 1k
Line / Space (μm)	30 / 20, 20 / 10	
Cu thickness (μm)	10 / 10 (1st / 2nd)	
Resin thickness (μm)	10 / 10 (1st / 2nd)	
Encapsulation layer(μm)	10	

Fig. 2 shows a schematic fabrication process representing the cross-section of the spiral inductor. These inductors were fabricated onto bare-Si wafer in this work, however this process can be applied with an actual wafer.

3. Result and Discussion

The evaluations were carried out by measuring DC resistance, Q and L of the fabricated inductor. Measurements of the inductors, open and short patterns, were carried out by

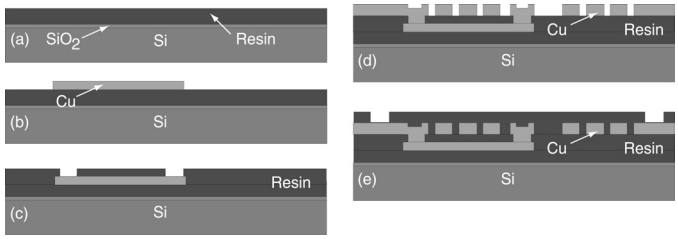

Fig. 2 Schematic cross-sectional diagram of the fabrication process.
(a) Resin coating and curing
(b) Formation of bottom conductive layer by Cu electroplating
(c) Photosensitive resin coating, patterning and curing
(d) Formation of upper conductive layer including coil patterns, grounds pattern and test pads by Cu electroplating.
(e) Encapsulation resin coating.

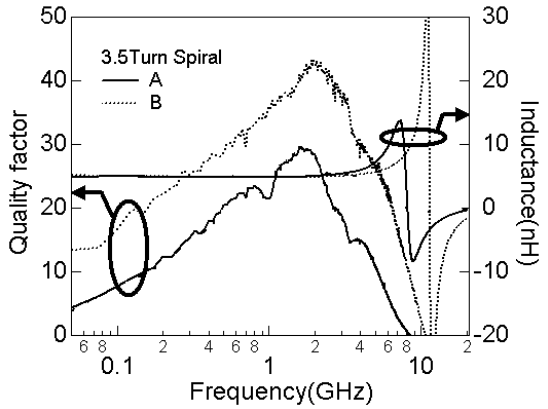

Fig. 3 Frequency dependence of L and Q in 3.5 turn spiral inductors without encapsulation layer.

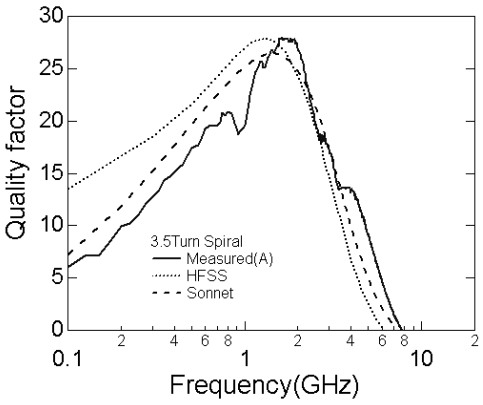

Fig. 4 Comparison between the measured results and simulated values in 3.5 turn spiral inductor with encapsulation layer.

a network analyzer to obtain S-parameter. Then, S-parameter of the inductor was de-embedded from the open and short patterns. The Q and L were derived from the following equations [3].

$$Q = \frac{-\mathrm{Im}\{Y_{11}\}}{\mathrm{Re}\{Y_{11}\}} \quad (1)$$

$$L = \frac{1}{2\pi f}\mathrm{Im}\{\frac{1}{Y_{11}}\} \quad (2)$$

Fig. 3 shows measured L and Q as a function of frequency. L of 5.0 nH for A-type with Q of 29.3 at 2 GHz with f_{res} of 8.5 GHz was obtained. The Q of A-type denoted higher than that of conventional on-chip inductor, which was usually limited 10 or less.

Meanwhile, L of B-type was 4.9 nH with Q of 42.9 at 2 GHz with f_{res} of 10.7 GHz and tended to be higher than that of A-type because of the higher ρ of Si substrate. Although the coil pattern of A-type and B-type was separated 20 μm from the substrate, the influence of the induced eddy current in Si substrate still existed and reduced Q and f_{res} in A-type.

Table II shows an influence of the encapsulation layer for L, Q and f_{res} in 3.5 turn spiral inductor in A-type. Because of the increase of capacitance at adjacent Cu lines of the inductor due to the encapsulation layer, L increased 3.8 % at 2 GHz, Q at 2 GHz and f_{res} decreased 8.5 % and 8.9 %, respectively. These results denote that the influence of the encapsulation layer was slightly affected to the characteristics of the inductor. In addition, different number of turns and types also showed the same tendencies.

Fig. 4 shows a comparison of the simulated Q by HFSS and Sonnet as a function of frequency with the fabricated result of the 3.5 turn spiral in A-type with encapsulation layer.

Table II
Influence of the encapsulation layer on L, Q and f_{res} in 3.5 turn spiral inductor in Type-A.

3.5 turn spiral inductor in Type-A	L at 2GHz (nH)	Q at 2GHz	f_{res}(GHz)
Without Encapsulation layer	5.0	29.3	8.5
With Encapsulation layer	5.2	27.0	7.8

The good correspondence between the fabricated result and the simulated results without the encapsulation layer has been reported in the previous work [4], in addition, this paper deals a comparison with the encapsulation layer. The differences in Q between the simulated values and the fabricated result at 2 GHz were 11.1 % and 8.9 % in HFSS and Sonnet, respectively. The deviations from different number of turns and types stayed within an accuracy of 15 % in terms of Q. Therefore, both of the simulated values were well corresponded to the fabricated results in every number of turns and types.

In other words, These electromagnetic simulators demonstrated that they were quite effective tools to design the on-chip spiral inductors on Si substrate as well as these inductors were integrated with WLP including thick resin layers and Cu conductors.

4. Conclusion

In order to achieve high performance passive components integrated with CMOS circuit, high-Q spiral inductors on Si substrate integrated with WLP have been successfully fabricated. The inductance L of 5.2 nH with the quality factor Q of 27.0 were obtained for a 3.5 turn rectangle spiral inductor with encapsulation layer at 2 GHz on the Si substrate, which had a resistivity of 4-6 Ωcm. In addition, the simulated results were well corresponded with the fabricated results.

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