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Small Area Snake Inductor on Si RF CMOS Chip

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I. Introduction

Importance of design and implementation of on-chip inductor is increasing in Si RF CMOS circuit, because the performance of passive components directly affect the circuit performance and chip cost. The on-chip inductor has been used as matching network component, baluns, inductive load, and so on. The requirements for on-chip inductor are (1) to have an appropriate inductance value, (2) high self-resonance frequency, (3) high-quality factor Q, and (4) small area on Si wafer. In this paper, we propose a novel ultra small area inductor on Si CMOS chip.

Figure 1 shows the conventional on-chip inductors. The inductance is substantially determined by the self inductance of each turn and mutual inductance among each turn. In the spiral inductor (Fig. 1(a)), large device area of $D\times W \approx$(sveral hudred μm)^2 is required for several nH, which is used in GHz application. Furthermore, the Si substrate loss degrade Q, so that the substrate engineering such as counter doping and ground shield technology [1] has been employed. For meander (Fig. 1(b)) and solenoid (Fig. 1(c)) inductors also require a relatively large area because of their small positive mutual inductance, e.g., $D = 1600\mu$m and $W = 68\mu$m is required for several nH solenoid inductor, which was fabricated using MEMS technology [2][3].

For improvement of Q, several approaches have been reported; use of multilevel interconnect structure [4], use of surface MEMS technology [2][3], use of redistributed layers [5]. However, the area of inductor is very large of several-hundred-μm square; the RF circuit suffers from the area penalty of large inductance area. For example, in the matching network application, small area size is required instead of high-Q. The snake type inductor proposed in this work features its small size with small effect of Si substrate loss.

II. Structure of Snake Inductor

Figure 2 shows a schematic structure of the proposed "snake inductor", which is a solenoid-like inductor using upper and lower metal layers of multilevel interconnect. The structural feature is a dense metal turns comparing to the simple solenoid inductor as shown in Fig. 1(c). The dense metal turns is attributed from (1) the use of top 2 metal layers of M5 and M4, and the use of lower 2 metal layer of M1 and M2, and (2) the snake type turn as shown in Fig. 2. The magnetic flux is parallel to the substrate, so that the substrate loss can be decreased. The plane view device area can be reduced dramatically; The most important feature is a dramatic reduction of plain view device area. Table I summarizes the performance of inductors, which have similar inductance value. The area of snake inductor is less than 1/20 of the conventional on-chip spiral inductor and solenoid inductor using MEMS.

III. Result and Discussion

Two types of snake inductor have been designed and fabricated using 0.18 μm 5-metal layer CMOS process. The line width w and space s are 5 μm and 1 μm, respectively. The length D are 270 μm for inductor A and 420 μm for inductor B. The plane view device are $D\times W$ are 270 μm $\times$ 11 μm and 420 μm $\times$ 11 μm. The characteristics of snake inductor are measured by a vector network analyzer (Agilent 8720ES) using GSG probe heads (Cascade). Figure 4 shows photomicrograph of test structure. For de-embedding of probe pads, the open and short pad structures are used. Figures 5 and 6 show measured inductance L and quality factor Q as functions of frequency. L of inductor A is 1.46 nH at 10 GHz, and L of inductor B is 2.09 nH at 5.25 GHz. L of inductor A is smaller than that of B because the total self and positive mutual inductance of inductor A is smaller than that of B. Q of inductor A is 1.76 at 10 GHz, and Q of inductor B is 1.13 at 5.25 GHz. The self-resonance frequency is 18.5 GHz in inductor A and 11.1 GHz in inductor B. Q and self-resonance frequency of the inductor B are smaller than those of inductor A due to difference of the parasitic capacitance between adjacent conductors and substrate loss. The self-resonance frequency of inductors are larger than 10 GHz.

IV. Conclusions

We have proposed a novel "snake inductor" on a Si CMOS chip, whose inductance is of nH-order for GHz applications. The device area is less than 1/20 of conventional on-chip inductors. The measured inductance is 1.46 nH and 2.09 nH. The quality factor is 1.76 and 1.13 respectively. The proposed inductor is suitable for the on-chip matching network, where the small area is required.

References

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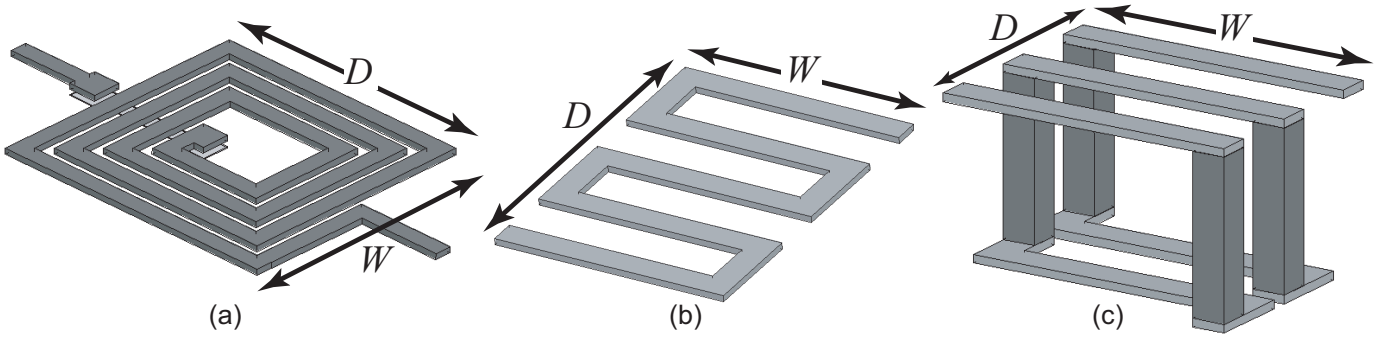

Fig. 1. Conventional on-chip inductors. (a) Spiral (b) Meander (c) Solenoid

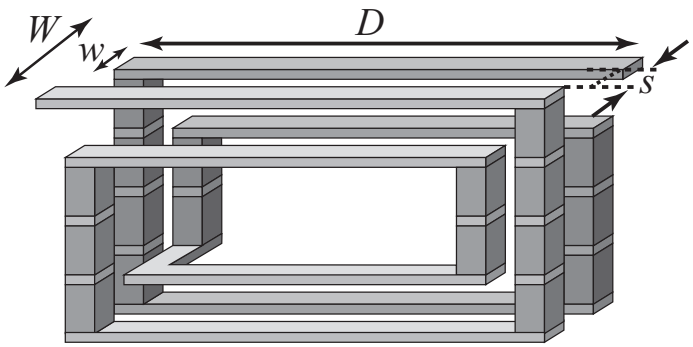

Fig. 2. Schematic structure of snake inductor.

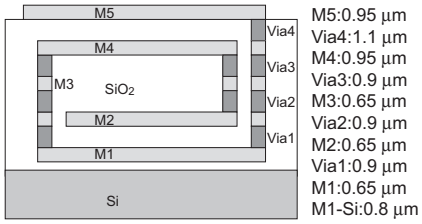

Fig. 3. Schematic cross section of multi-level interconnect structure.

TABLE I
COMPARISON OF INDUCTORS

	Spiral [6]	Solenoid (MEMS) [3]	This Work (A)	This Work (B)
f [GHz]	3.1	2.4	10.0	5.25
L [nH]	2.24	2.67	1.46	2.09
Q	12	16.7	1.76	1.13
Area [μm^2]	300×300	1600×68	270×11	420×11

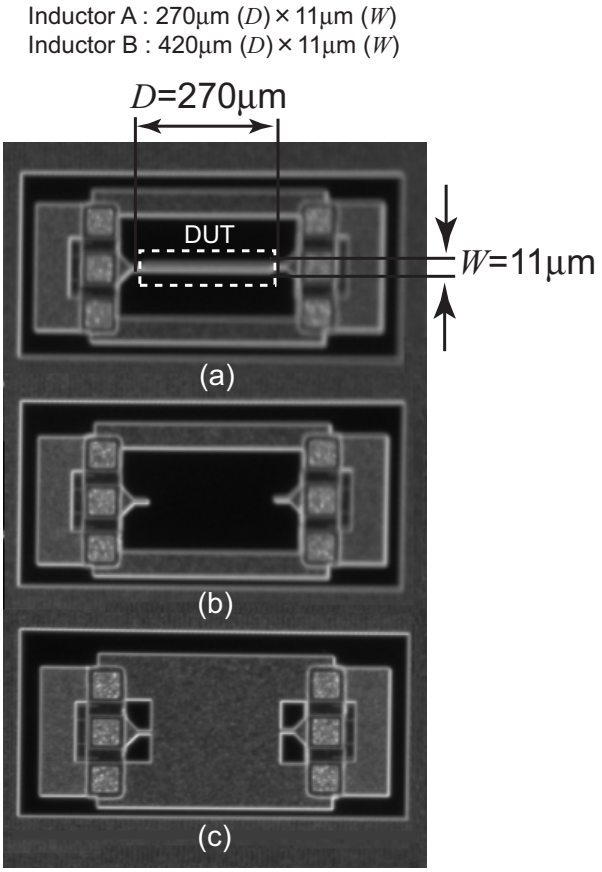

Fig. 4. Photomicrograph of test structure. (a) DUT with pad. (b) Open pad. (c) Short pad.

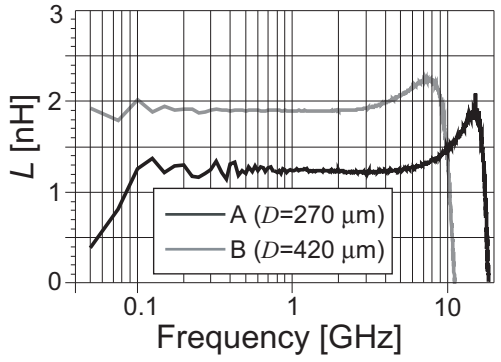

Fig. 5. Frequency dependence of the inductance $L = \frac{1}{\omega}\,\mathrm{I_m}\left(\frac{1}{Y_{11}^{\mathrm{ind}}}\right)$

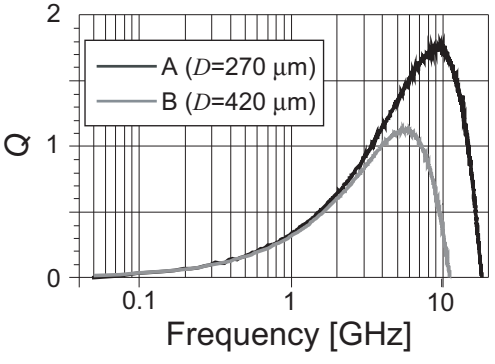

Fig. 6. Frequency dependence of the quality factor $Q = -\dfrac{\mathrm{I_m}\left(Y_{11}^{\mathrm{ind}}\right)}{\mathrm{R_e}\left(Y_{11}^{\mathrm{ind}}\right)}$