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Twisted Differential Transmission Line Structure for EMI Noise Reduction at Global Interconnect in Si LSI

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1. Introduction

EMI (electromagnetic interference) suppression is essential to high-speed electronic system design [1]. In Si LSI, EMI noise is produced by an interconnect [2], because interconnects have large characteristic impedance caused by uncertain current return pass. Since a wavelength of GHz signal is comparable to a length of global interconnect due to increase of clock frequency, the global interconnect has a potential to act as an antenna. Thus, EMI noise from global interconnects becomes crucial in signal integrity.

This paper proposes a twisted differential transmission line structure as a global interconnect to reduce EMI noise. If a global interconnect is designed as a transmission line, electromagnetic field is confined in the transmission line. The differential transmission line can transmit low-voltage signal because of high crosstalk-robustness of differential line. Thus, the differential transmission line has a capability for EMI noise reduction rather than the single-ended transmission line which employs rail-to-rail voltage. Additionally, the differential transmission line can achieve both high-speed signal transmission and low power consumption as compared to the conventional RC interconnects [3]. The present paper describes the EMI-noise reduction capability of the twisted diagonal-pair line interconnect.

2. Characteristics of Diagonal-Pair Line

Figure 1 (a) shows a cross section of the diagonal-pair line structure which can reduce both the crosstalk noise and interconnect resource [3]. AMS 0.35 μm CMOS process parameters are used for interconnect. Interconnect structure consists of three metal layers (aluminum). The thickness of metal 3 layer is 0.9 μm, and thicknesses of metal 2 and 1 layers are 0.6 μm. The thickness of ILD (silicon dioxide) is 1.0 μm. The interconnect has width of 4.0 μm, line space of 2.6 μm, and differential impedance $Z_{\rm diff}$ of 100 Ω. Figure 1 (b) shows measured eye-patterns of the 3 mm-long diagonal-pair line. The interconnect can transmit 12 Gbps pulse signal.

A three-dimensional electromagnetic simulation (CST, MW Studio) and a circuit simulator (Agilent, Advanced Design System) are used for time-domain waveform generation. Figure 2 shows the simulation condition. Differential pseudo random bit sequence (PRBS) is inputted to the differential transmission line that has length of 1 cm. The voltages of PRBS are 0.30 Vp-p. Eye-diagrams are generated using differential output waveforms (OUT, $\overline{\rm OUT}$).

Figure 3 shows the simulated eye-patterns of one-cm-long diagonal-pair line at 10 Gbps. The M1 line has larger attenuation than the M3 line as shown in Figs. 3 (a) and (b), because the M1 line is influenced by Si substrate loss more than the M3 line. Thus, the common-mode noise is generated due to unbalance of attenuation as shown in Fig. 3 (d). The common-mode voltage is 0.08 Vp-p and produces EMI noise. However, the power of EMI noise can be reduced 27 dB compared to conventional global interconnect that has the signal voltage of 1.8 Vp-p. The common-mode current generates much larger electromagnetic radiated emission and crosstalk noise more than the differential-mode current. It is important for GHz LSI to reduce common-mode current in global interconnect.

3. Low EMI-Noise Interconnect

Figure 4 shows proposed twisted diagonal-pair line structure. The twisted line structures were discussed to reduce crosstalk in bit lines of DRAM [4]. We propose the twisted line for EMI noise reduction at global interconnect on Si LSI. High crosstalk-robustness and interconnect-density bus line can be achieved using twist method as shown in Fig. 4 (c). The losses at twist parts are much smaller than that of the whole line, because the length of twist part is only about 10 μm as shown in Fig. 4 (b).

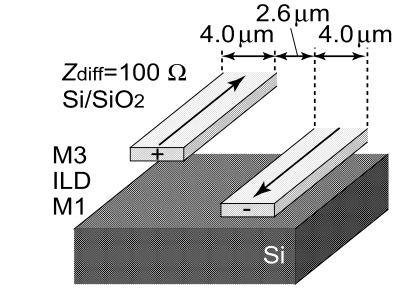
The twisted line averages losses on under and upper layer lines as shown in Figs. 5 (a) and (b). The twisted diagonal-pair line makes it possible to reduce the common-mode power of 20 dB compared to the normal diagonal-pair line. Compared to the conventional global interconnect, the common-mode power of 47 dB can be reduced. EMI noise can be dramatically reduced by the proposed twisted-diagonal-pair line on global interconnects.

4. Conclusion

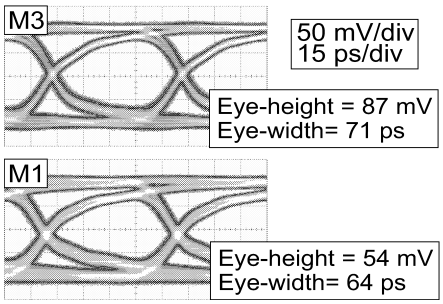
This paper has proposed the twisted diagonal-pair line for reduction of the EMI noise in LSI. The normal diagonal-pair line has smaller common-mode power than the single-ended global interconnect. The proposed twisted-diagonal-pair line can drastically reduce the common-mode power of 47 dB compared to the single-ended interconnect.

References

[1] K. Shimazaki, *et. al.*, Proc. IEEE ISQED, pp. 129–136, March 2000.
[2] H. Tsujikawa, *et. al.*, Proc. IEEE CICC, pp. 299–302, May 2002.
[3] H. Ito, *et. al.*, IEICE Trans. Electron., vol. E87–C, no. 6, June 2004, to be published.
[4] H. Hidaka, *et. al.*, IEEE J. Solid-State Circuits, vol. 24, no. 1, pp. 21–27, Feb. 1989.



(a) Cross section.



(b) Measured eye-patterns at 12 Gbps.

Fig. 1: (a) The diagonal-pair line structure. (b) Measured eye-patterns of the 3 mm-long diagonal-pair line.

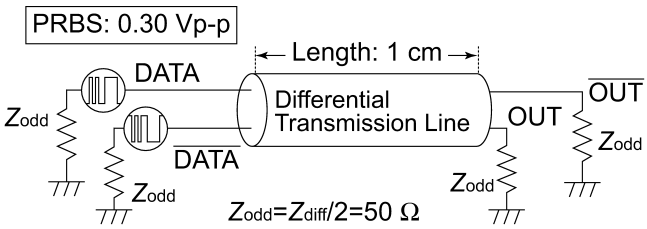
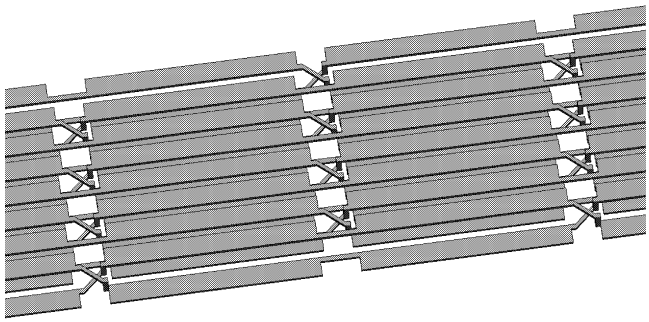
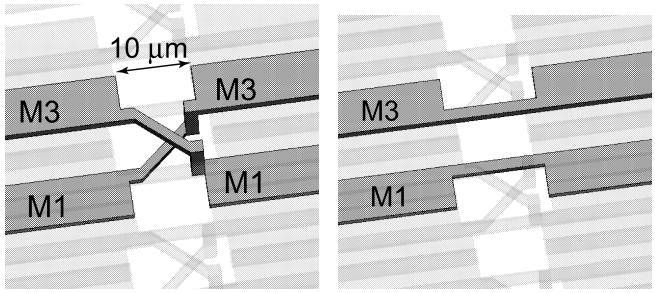


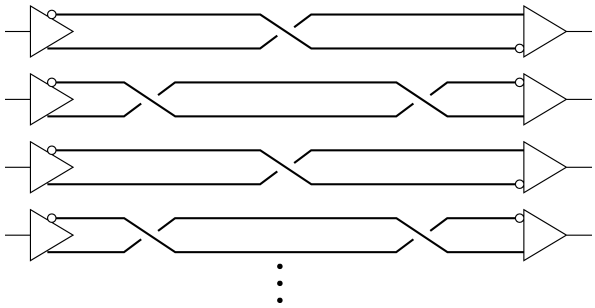
Fig. 2: ADS simulation condition.



(a) Bus line structure.

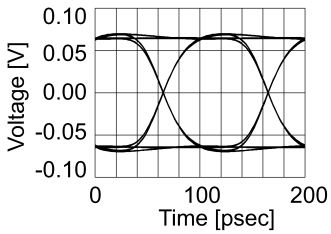


(b) Structure of twist part.

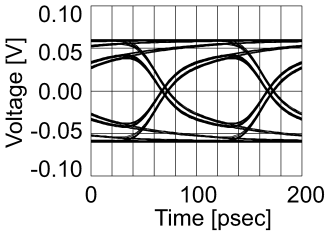


(c) Schematic of bus line.

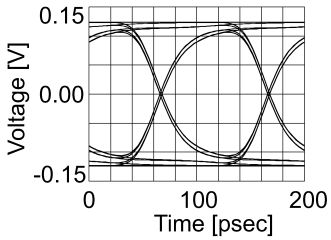
Fig. 4: The twisted diagonal-pair line structure.



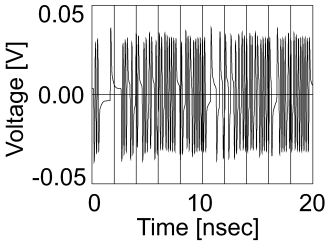
(a) M3 line.



(b) M1 line.

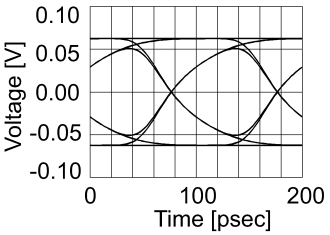


(c) Differential mode.

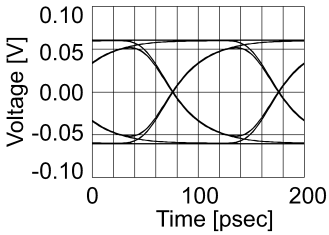


(d) Common mode.

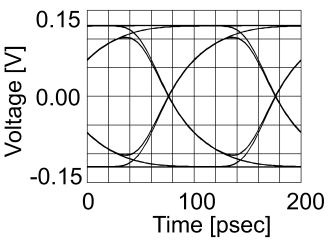
Fig. 3: Eye-patterns and wave-form of one-cm-long line at 10 Gbps.



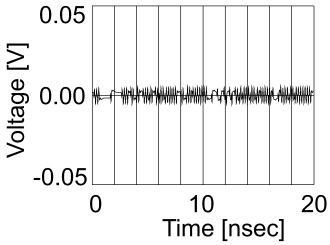
(a) M3 line.



(b) M1 line.



(c) Differential mode.



(d) Common mode.

Fig. 5: Eye-patterns and wave-form of one-cm-long twisted line at 10 Gbps.